FPGA processing for High Performance Computing

Prabu Thiagaraj, Benjamin Stappers, Jayanta Roy, Michael Keith, Mitchell Mickaliger

Jodrell Bank Centre for Astrophysics,
School of Physics and Astronomy, University of Manchester, UK

prabu.thiagaraj.manchester.ac.uk Ben.Stappers@manchester.ac.uk jayanta.roy@manchester.ac.uk
mkeith@pulsarastronomy.net mitch.mickaliger@gmail.com

SKA SQUARE KILOMETRE ARRAY

30 June – 1 July 2015

Abstract

Field Programmable Gate Arrays (FPGAs) are fine-grained, massively parallel, digital logic arrays with architecture suitable to execute computations in parallel. Although FPGAs have been in existence for more than two decades and known for their inherent ability to perform fine grain parallel processing tasks very efficiently, it is only in the last couple of years we could see the realization of their potential in the high-performance computing world. This transformation is mostly due to the recent and radical progress in the FPGA development tools and in the hardware technology. The talk outlines this evolution, touches upon the specific tools and vendor technologies that made the transformation possible and attractive. The second half of the talk will present how this new technology appears attractive especially due to the power efficiency for a signal processing application in radio astronomy, namely for the Square Kilometre Array (SKA) that we are involved in developing at the Jodrell Bank Centre for Astrophysics, School of Physics and Astronomy, University of Manchester.

Terms

FPGA - Field Programmable Gate Arrays

SKA - Square Kilometre Array

A new radio telescope being designed
It will be located in SA and Australia

Pulsar - A star with extreme nature

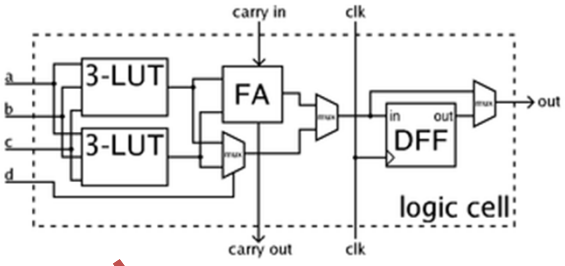
Rapidly rotating, made of neutrons
telescopes would pick series of regular pulses.

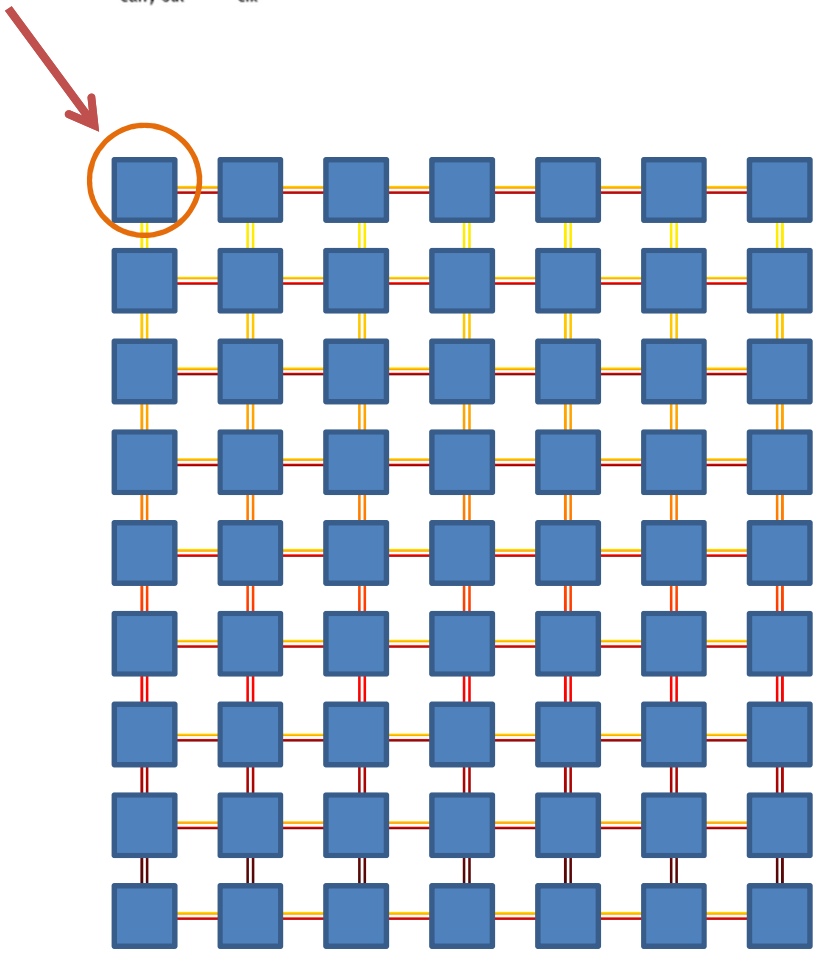
HPC - High performance computing

Trademarks:

ALTERA® , XILINX®, NALLATECH®, KHRONOS ®

Introduction





FPGA Architecture

Digital logic - ALU

Massive Array - 2D

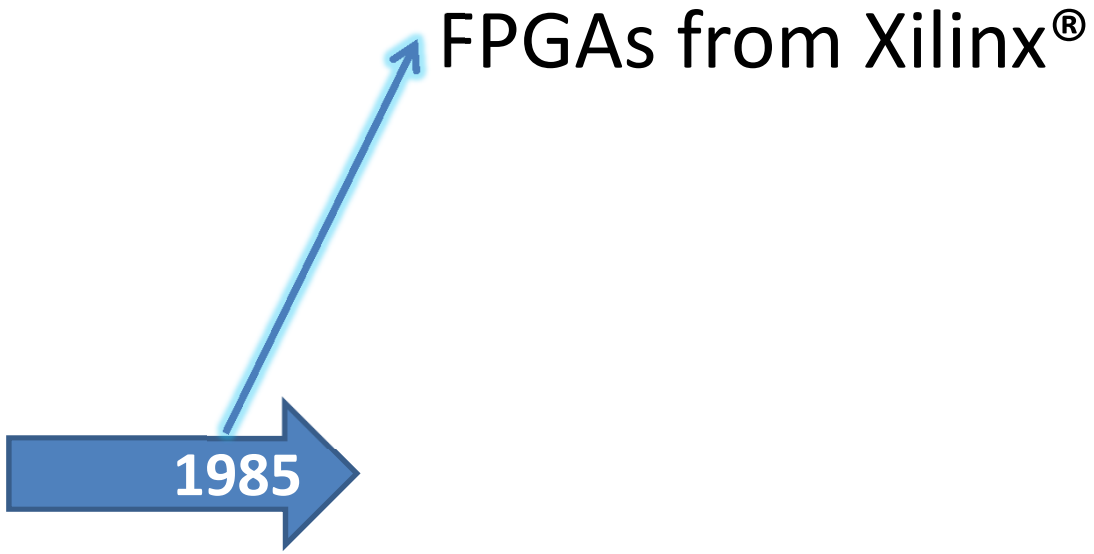
Impressive order

Extreme inter-connectivity

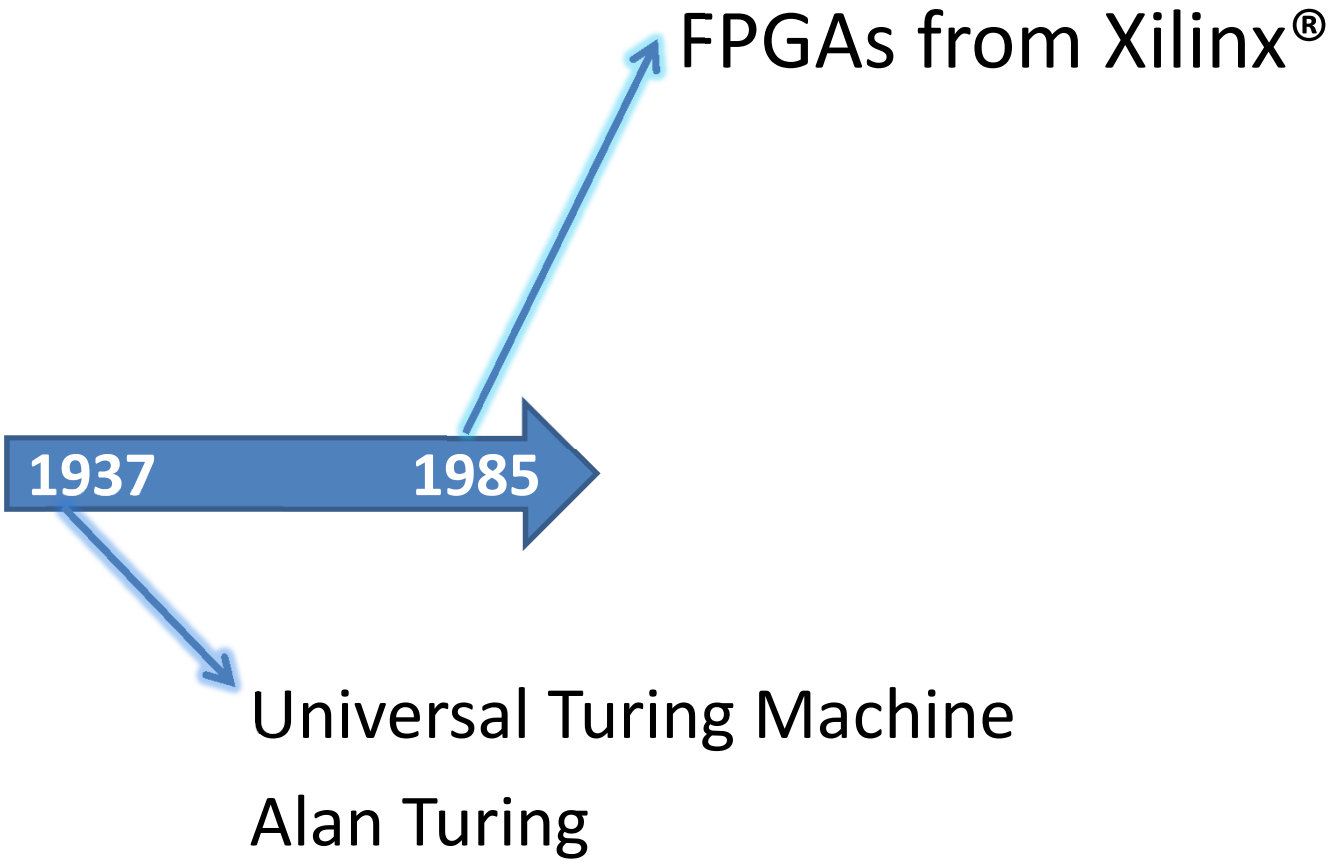
Parallel Operation

http://worrydream.com/dbx/

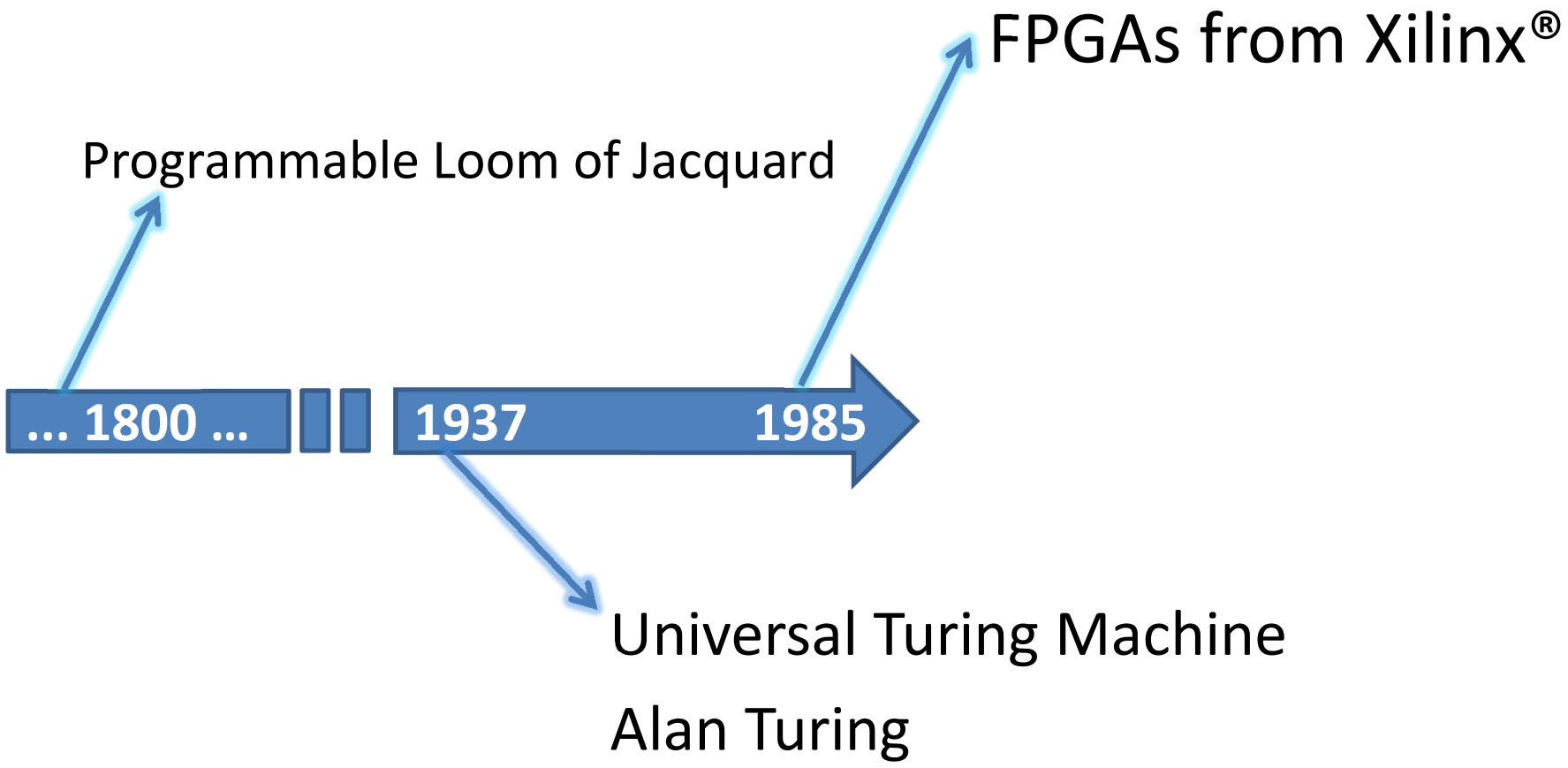
Away from traditional approaches



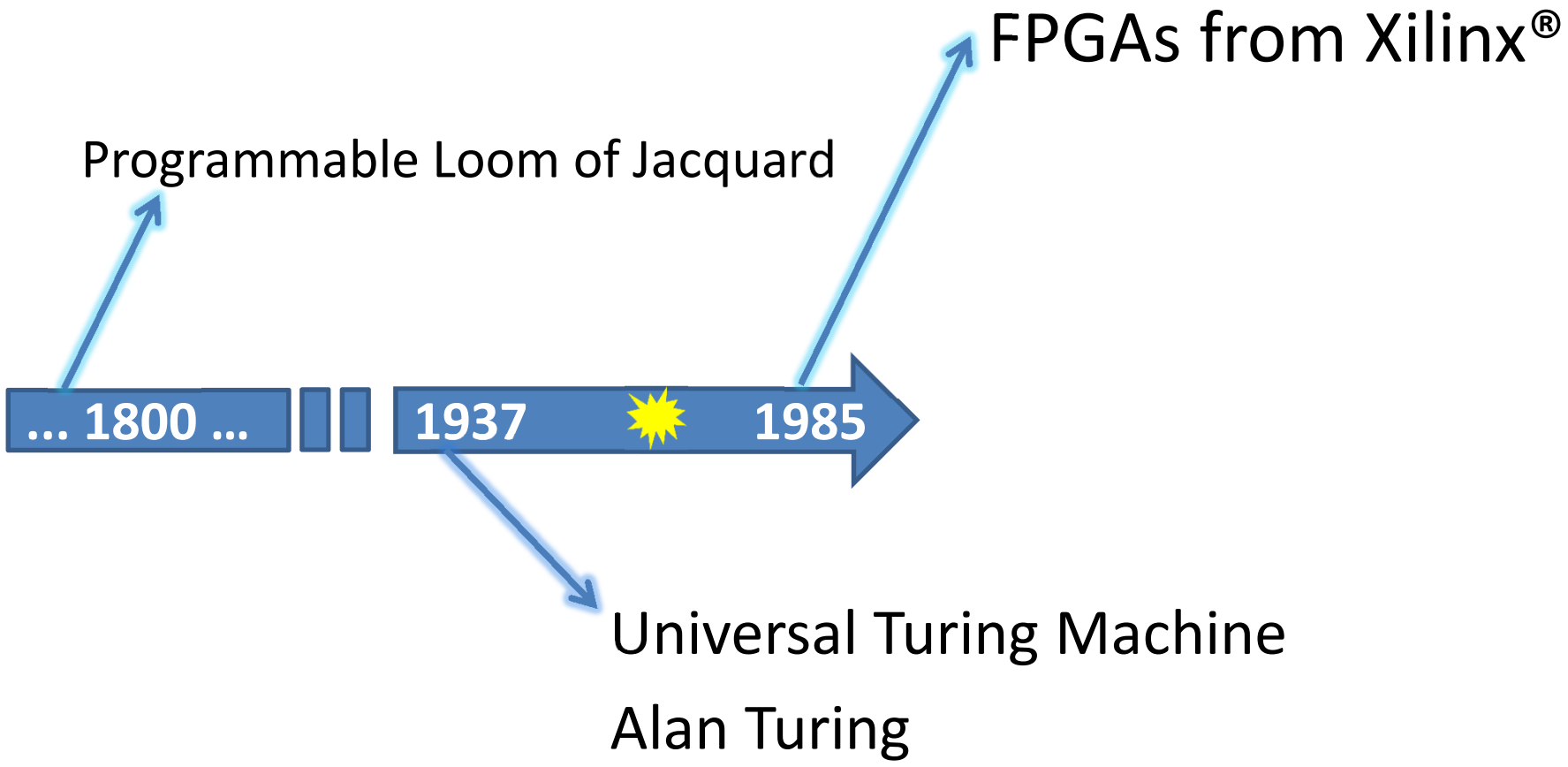
Away from traditional approaches



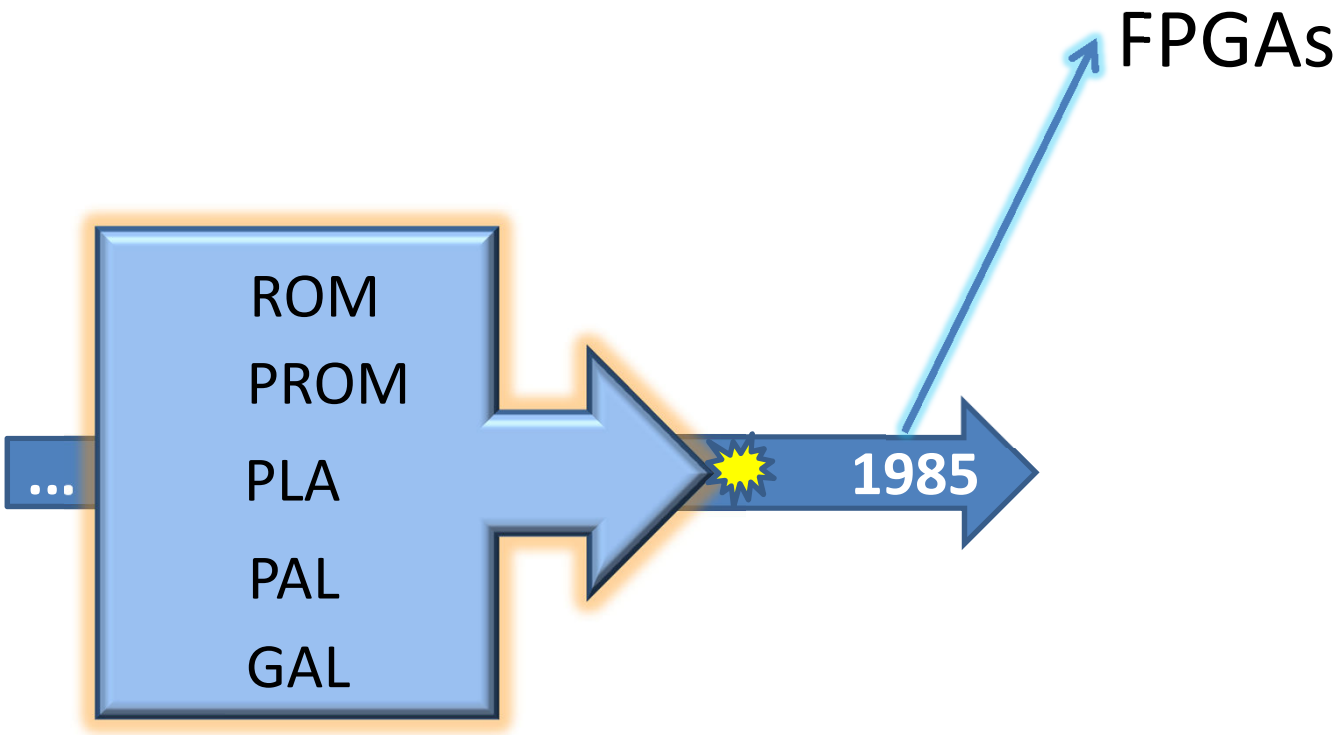
Away from traditional approaches



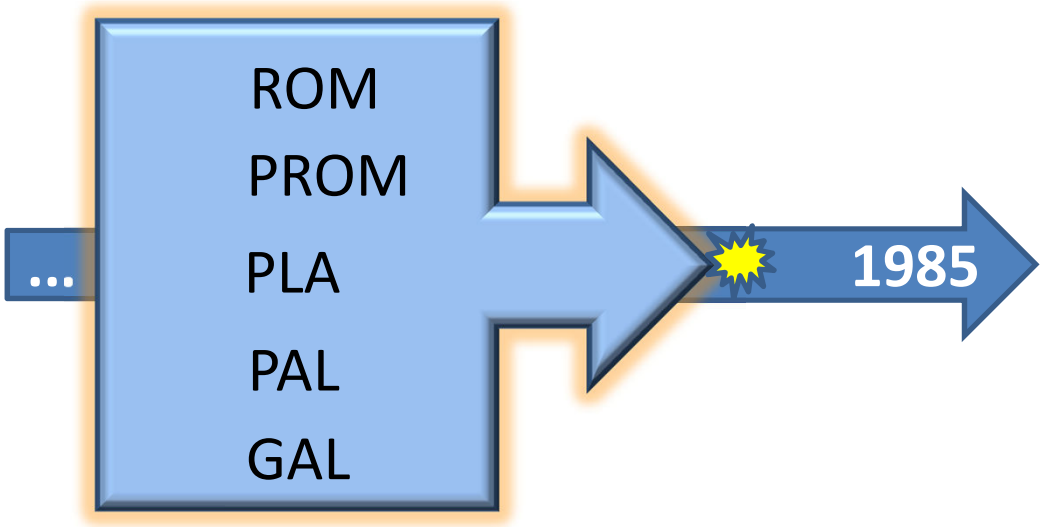
Away from traditional approaches



Away from traditional approaches



Away from traditional approaches

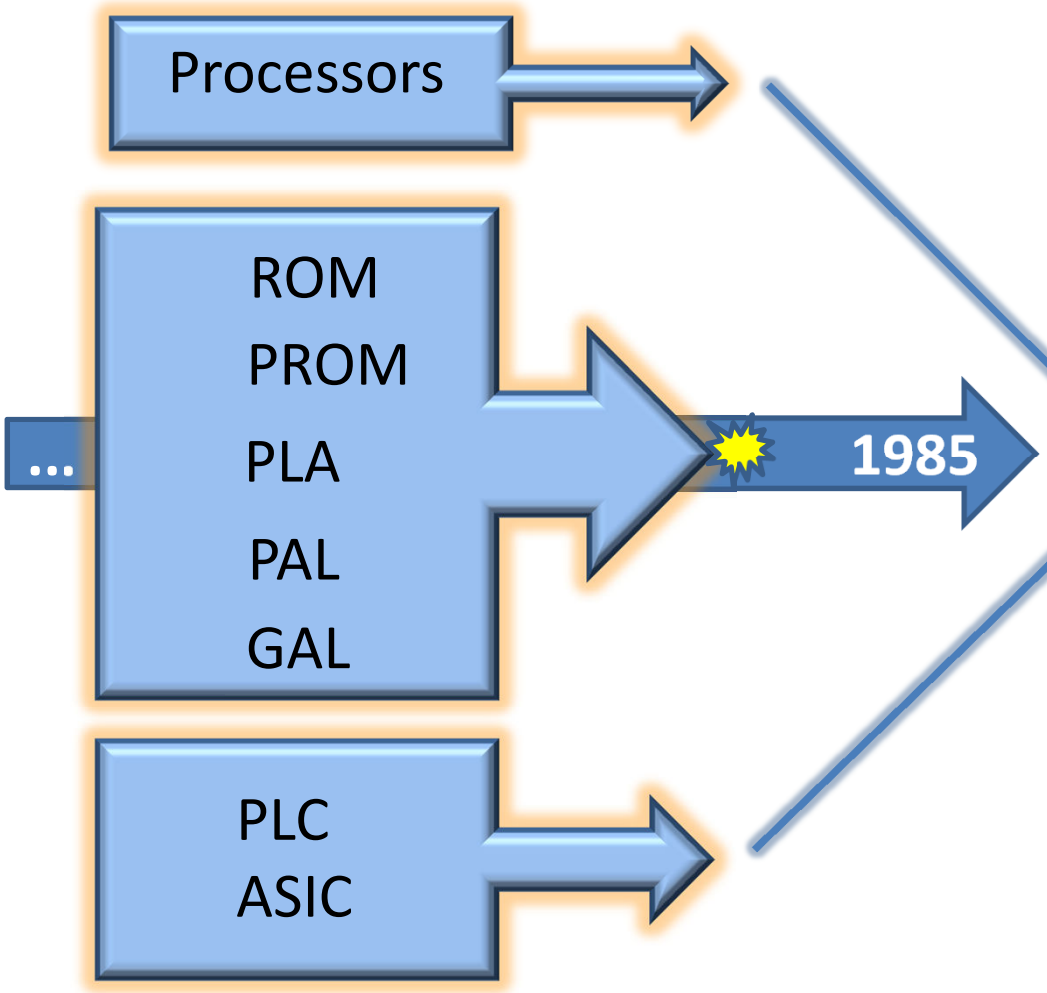


FPGA based Design

Modified the Traditional Circuit design

Tools: Design capture
Analysis & Synthesis
Fit & Route
Verification

Away from traditional approaches

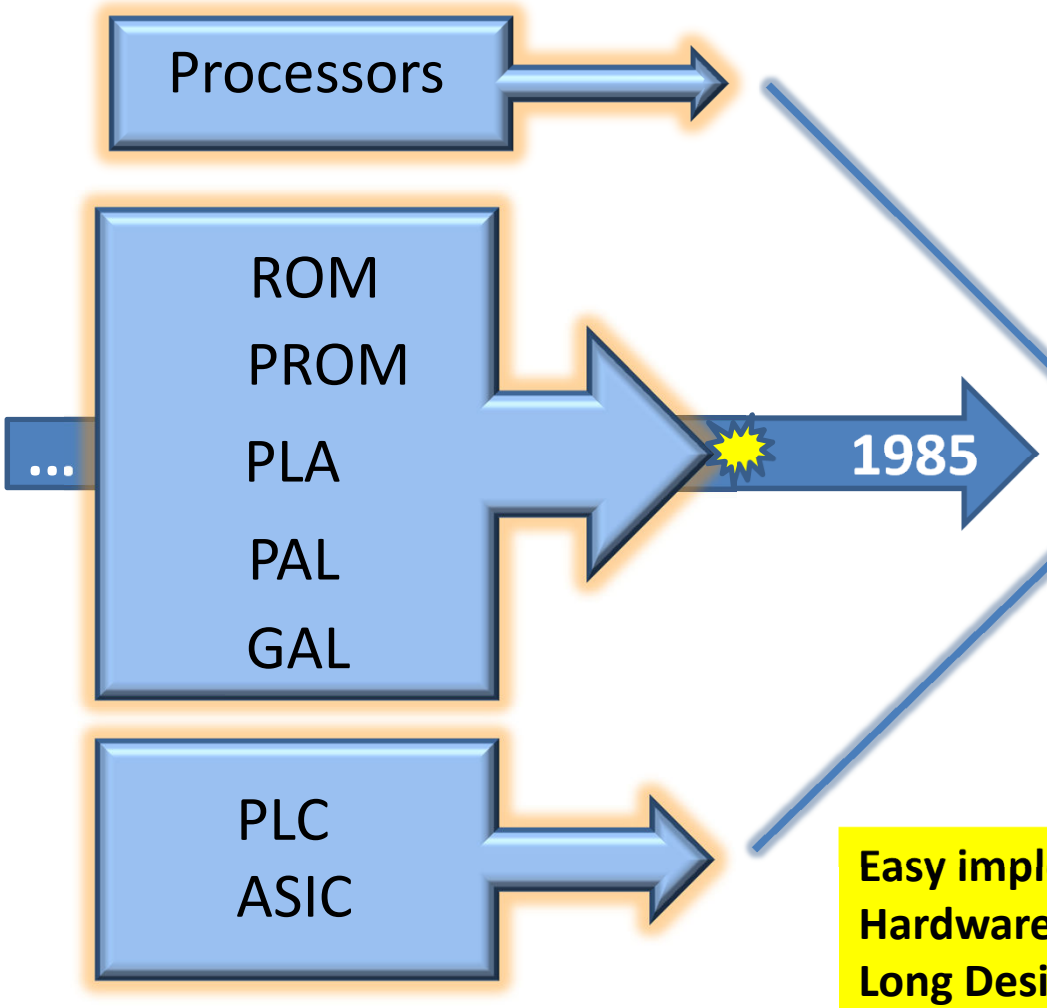


FPGA based Design

Modified the Traditional
Circuit design

Tools: Design capture
Analysis &
Synthesis
Fit & Route
Verification

Away from traditional approaches



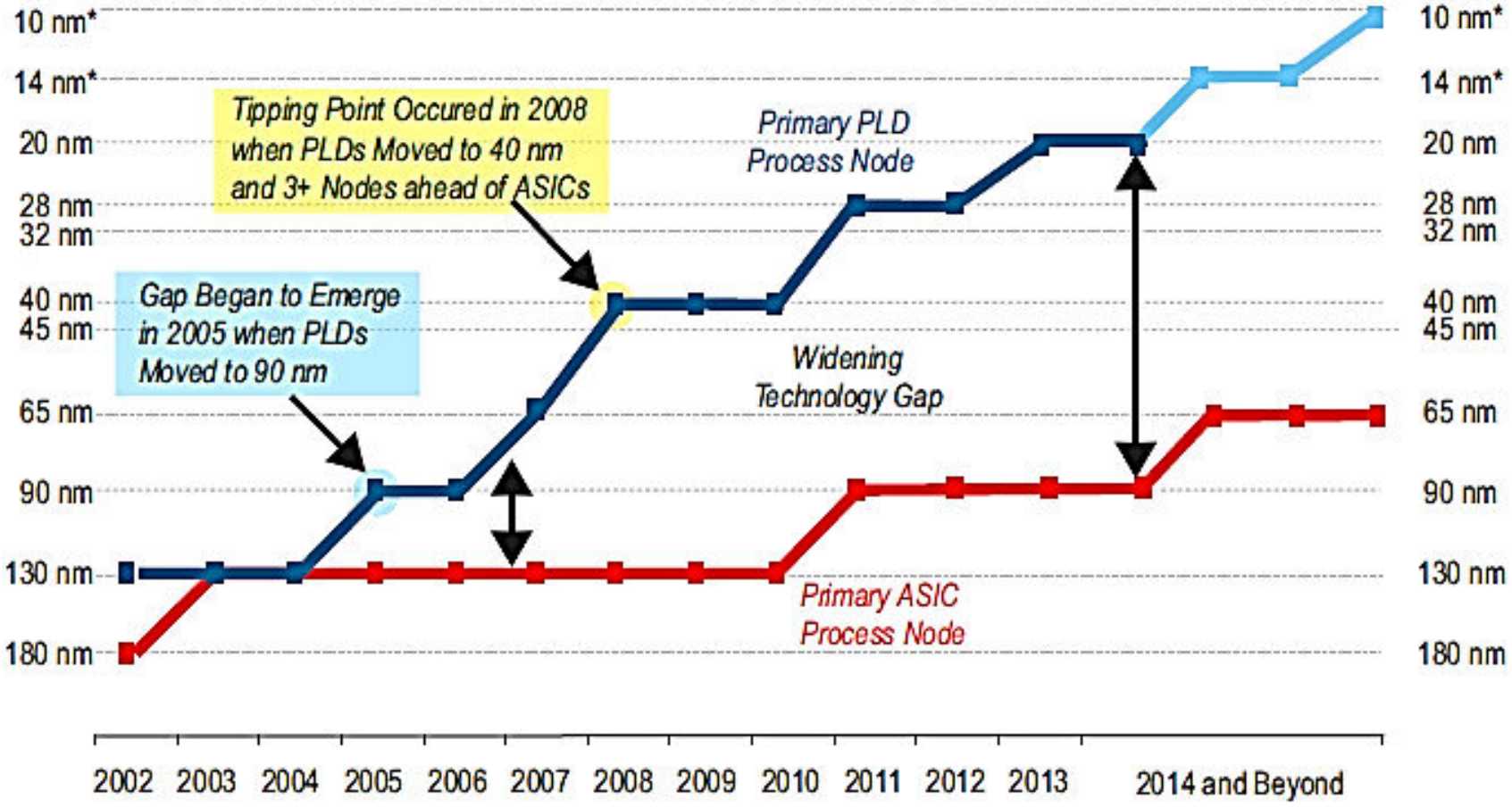
FPGA based Design

Modified the Traditional Circuit design

Tools: Design capture
Analysis & Synthesis
Fit & Route
Verification

Easy implementation for Complex circuits
Hardware Knowledge essential
Long Design Cycle. Worked well for small FPGAs

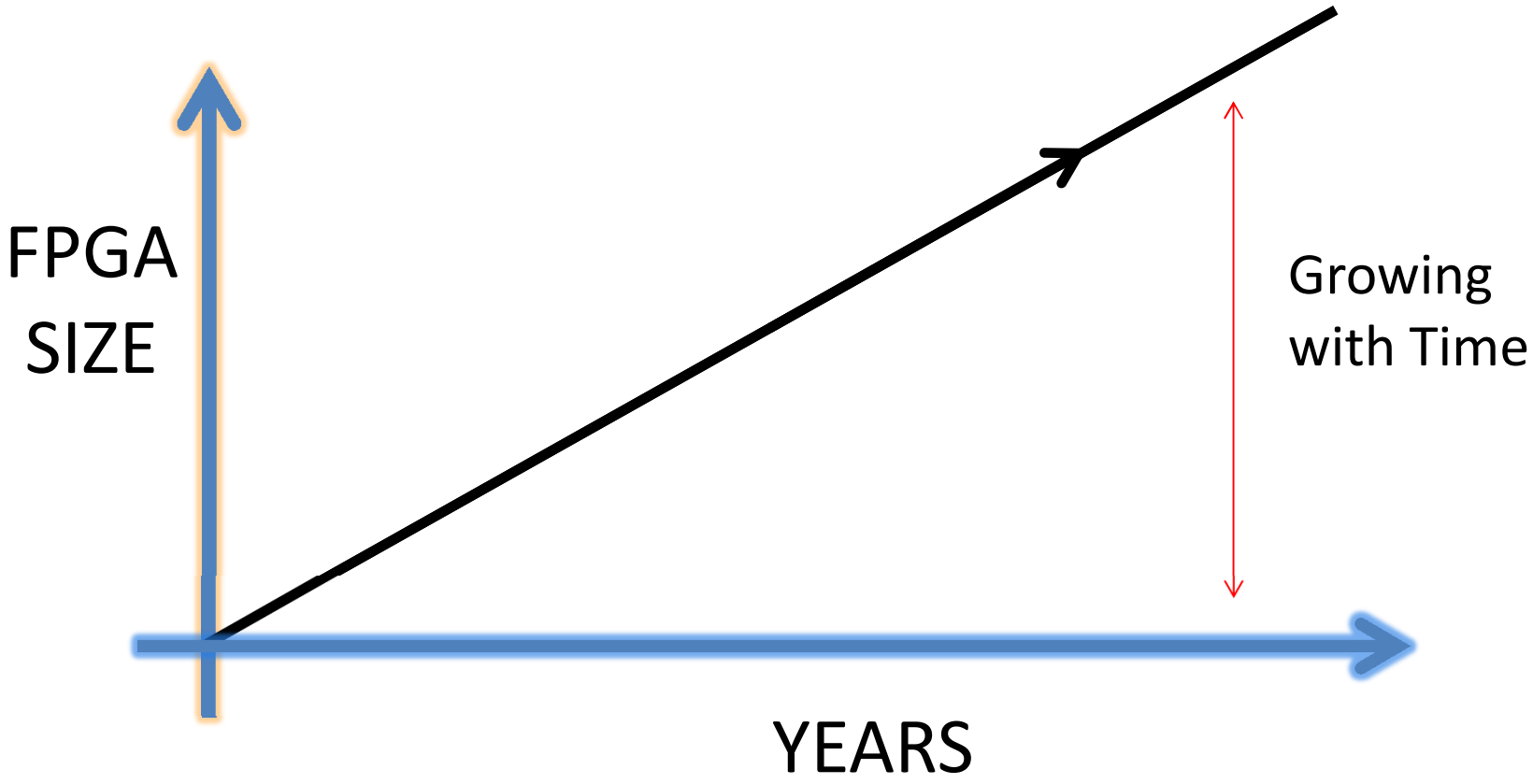
FPGA fabrication process (PLD) compared with that of ASIC



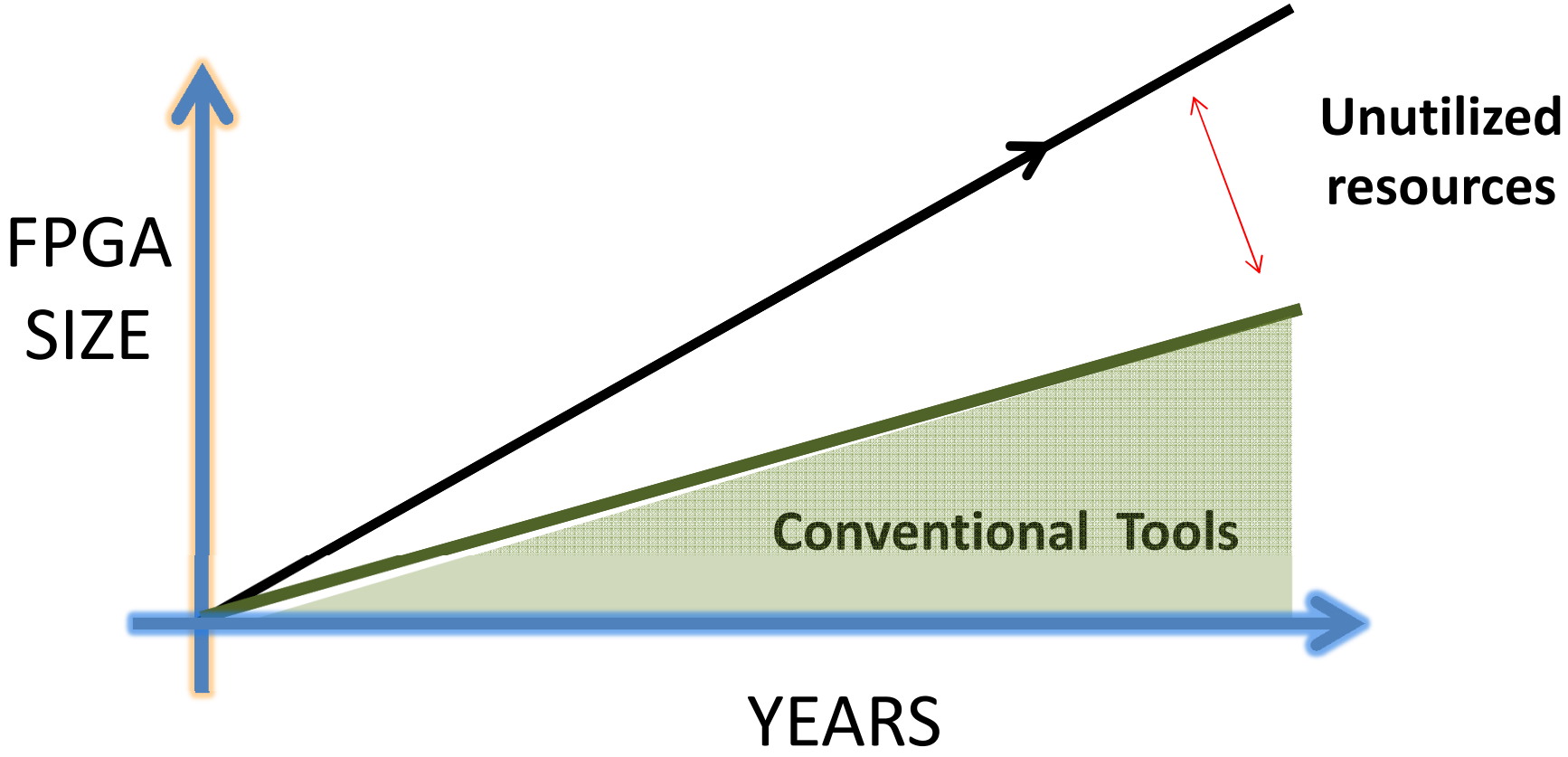
Source: Altera; Data applies to new design starts.

** FinFET Technology. Timeframe for PLDs on 14 nm and 10 nm FinFET technology to be announced.*

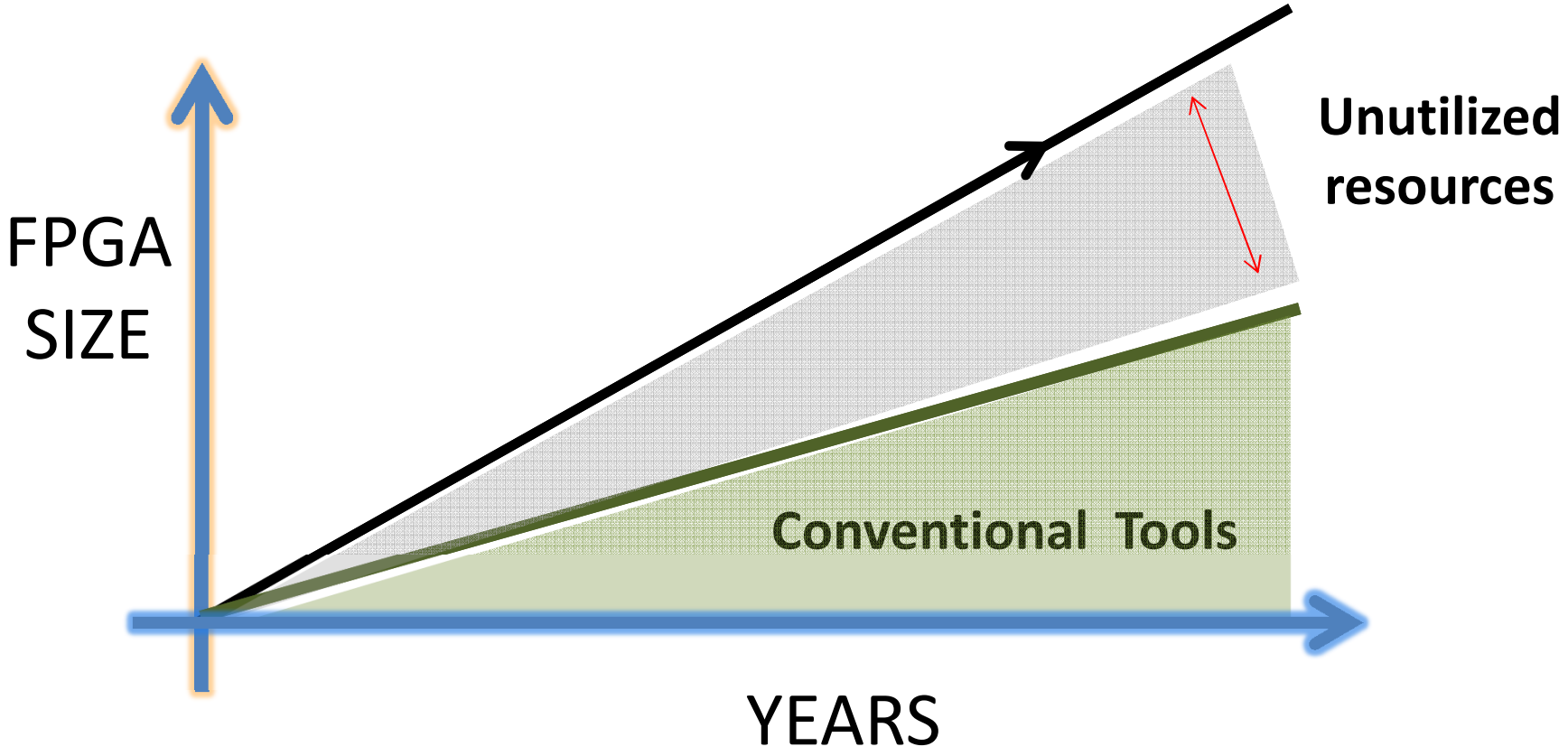
FPGA size increases
But can I use the entire FPGA ?



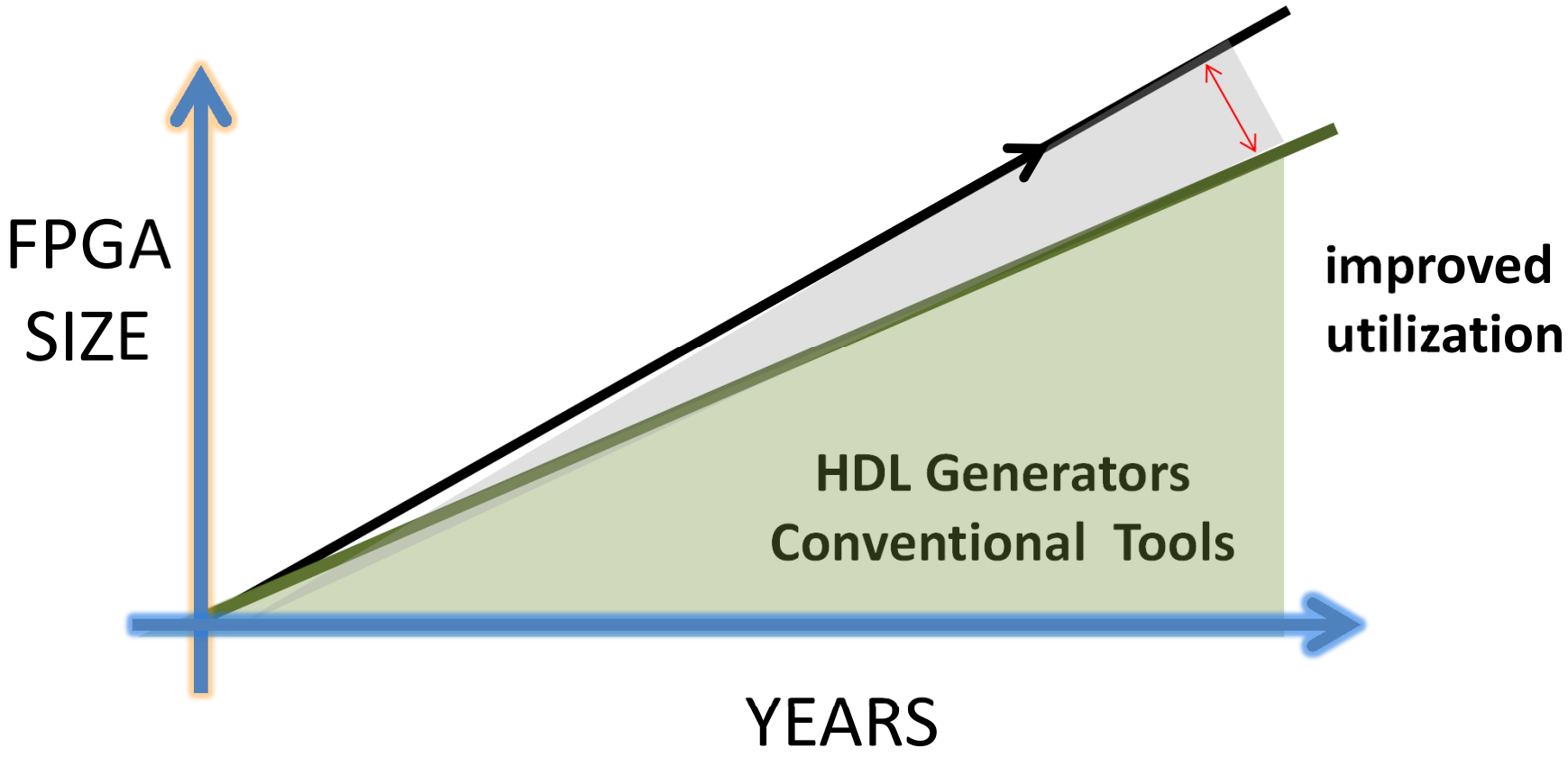
Can I use the entire FPGA ?
Use of Conventional Tools



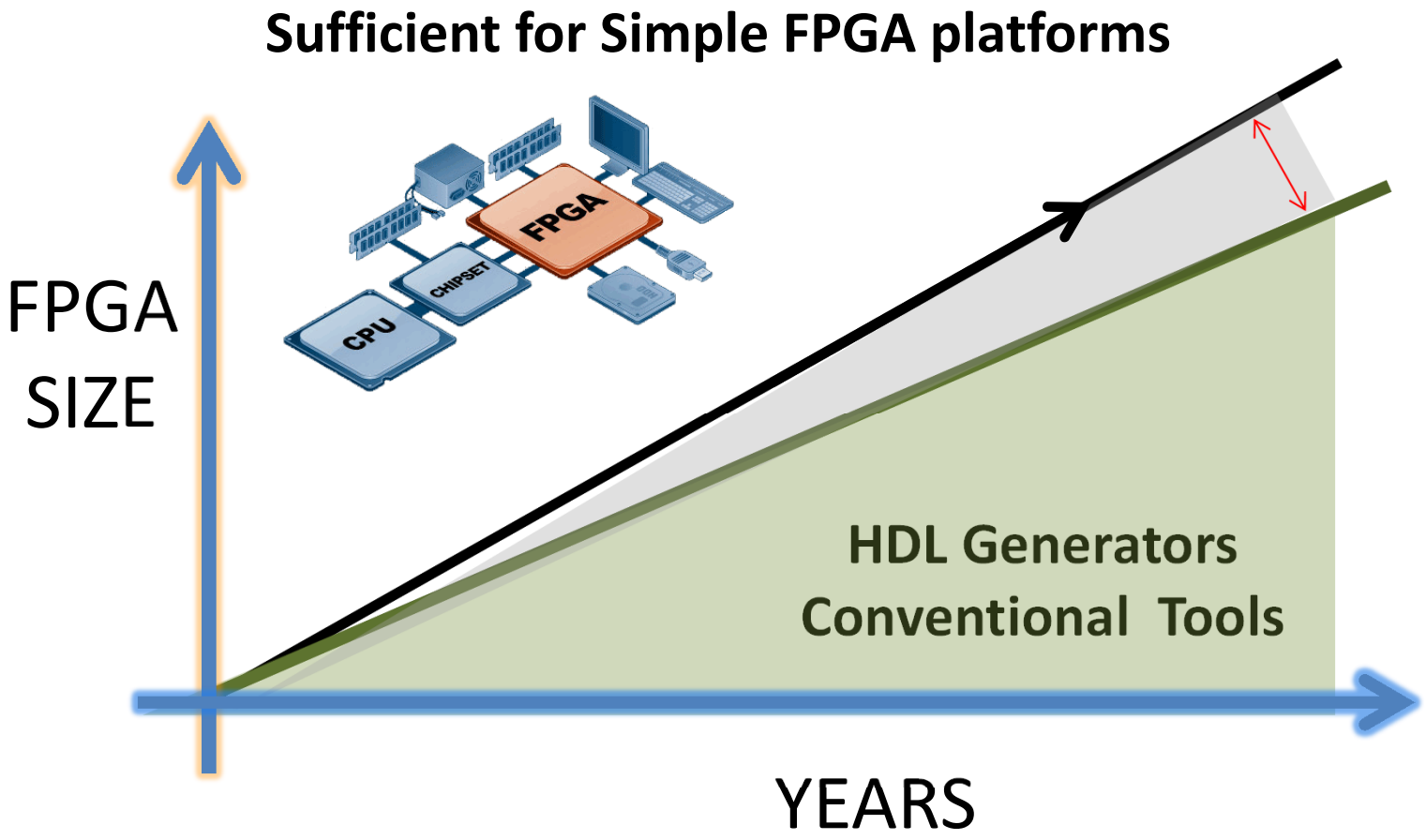
Can I use the entire FPGA ?
Dark resources - a challenge



Can I use the entire FPGA ?
HDL Generators – a solution



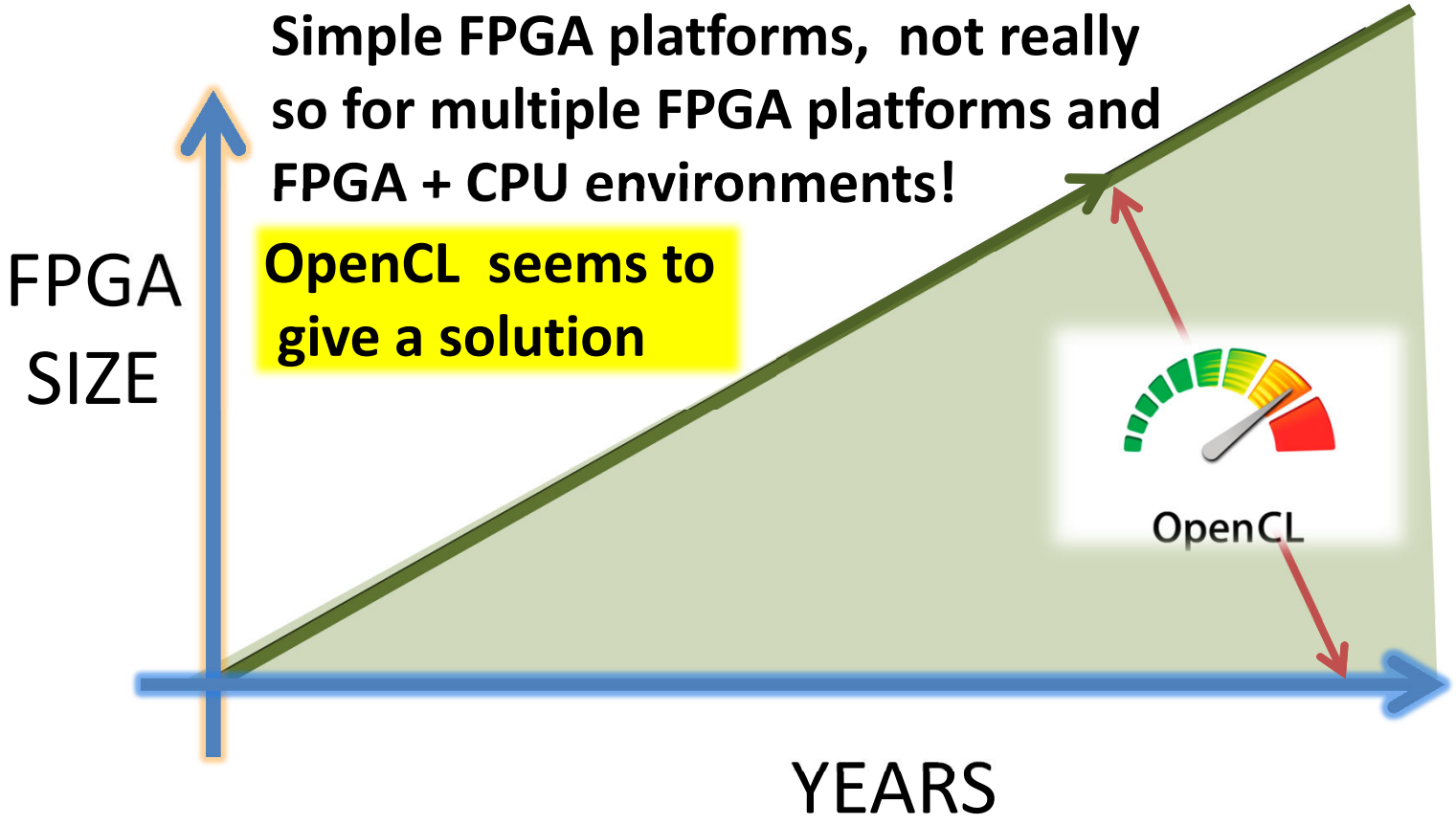
Can I use the entire FPGA ?
HDL Generators – a solution



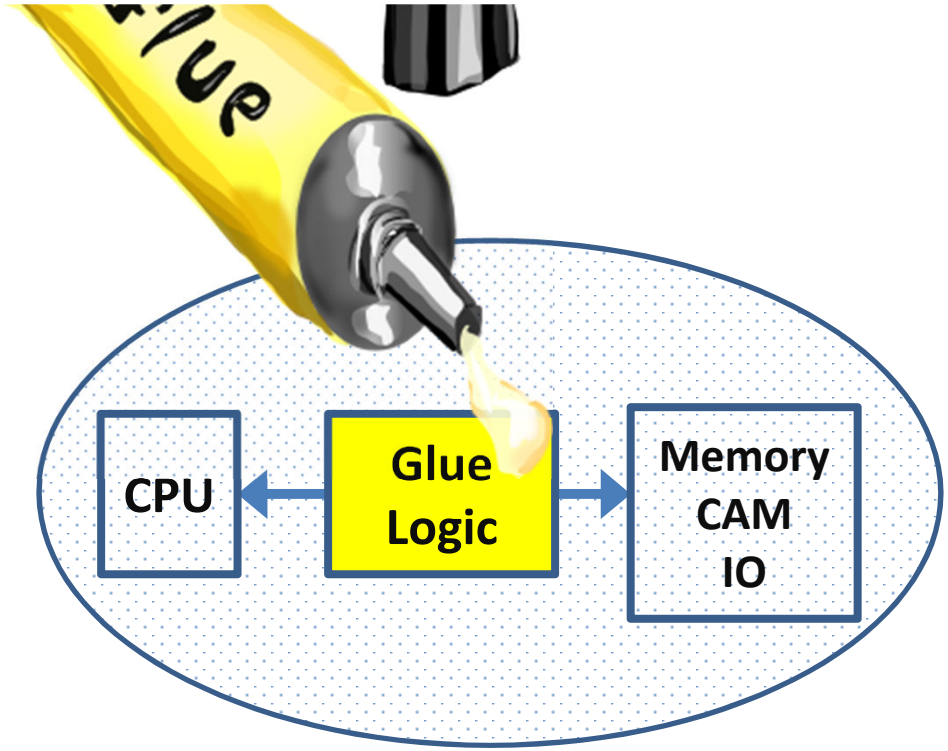
Conventional HDL Generators and Heterogeneous environments

While appeared sufficient for Simple FPGA platforms, not really so for multiple FPGA platforms and FPGA + CPU environments!

OpenCL seems to give a solution



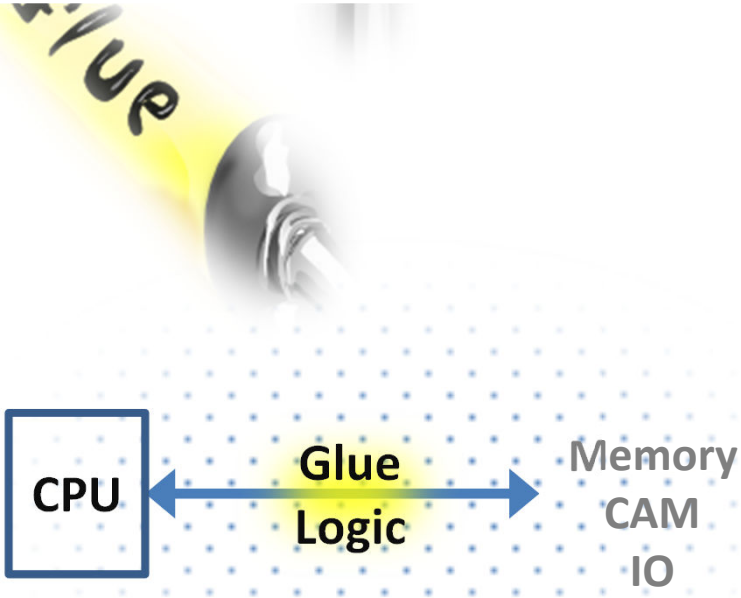
Role



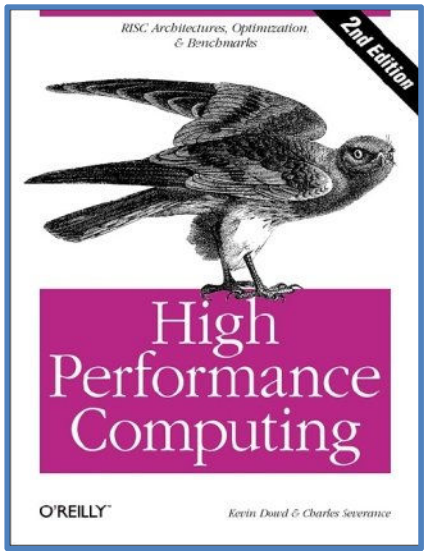
EARLY DAYS

Handy solutions for simple digital circuitry

Role Shift

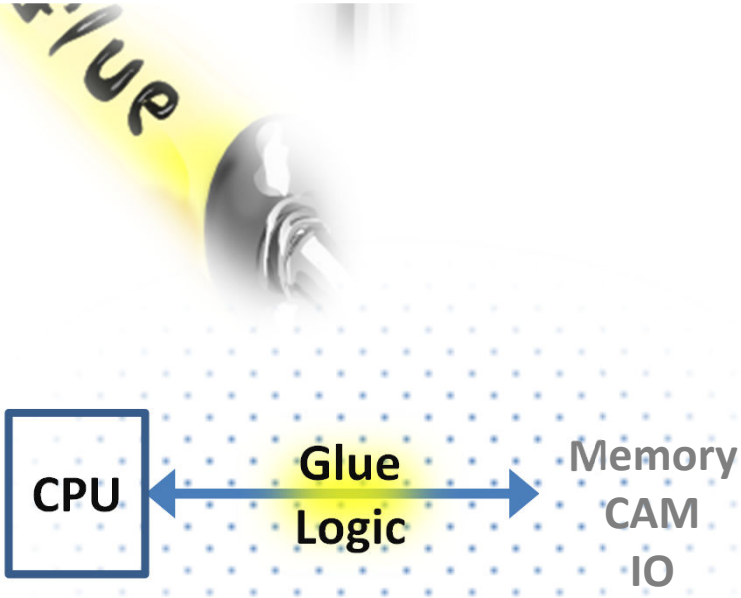


EARLY DAYS → **NOW**

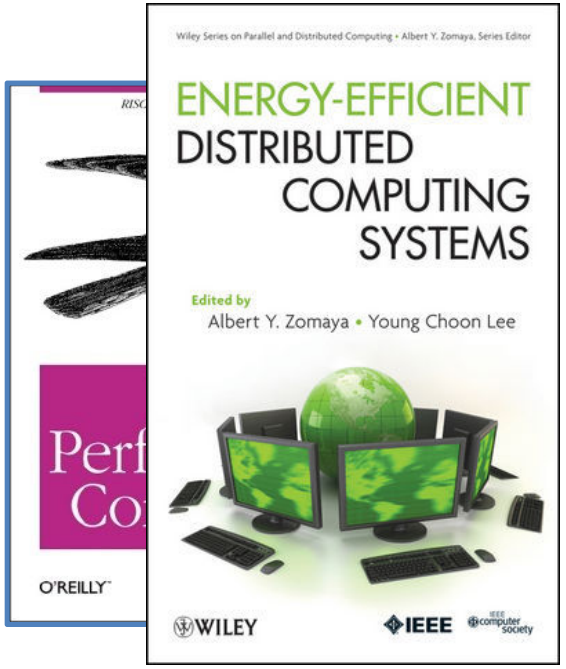


Handy solutions for simple digital circuitry
High Performance Computing

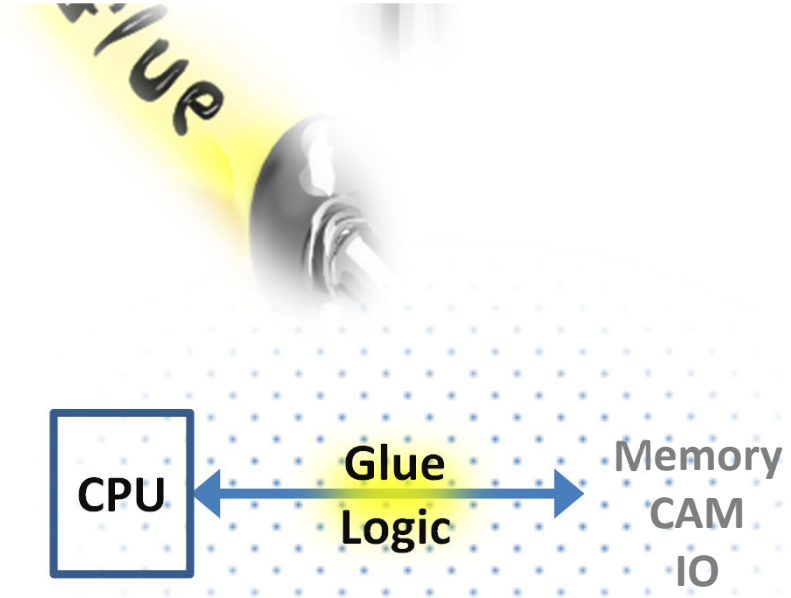
Role Shift



EARLY DAYS → **NOW**



Handy solutions for simple digital circuitry
High Performance Computing
Energy-efficient solutions



Role Shift

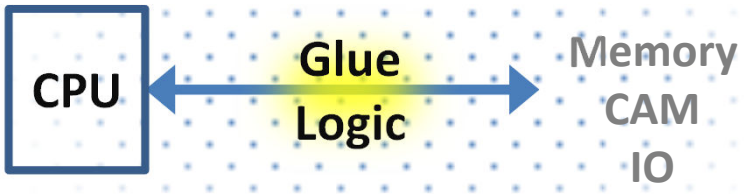
Matured FPGA Development Tools
Electronic Design Automation
and a radical approach in adapting to
Host-device programming using OpenCL

EARLY DAYS → **NOW**

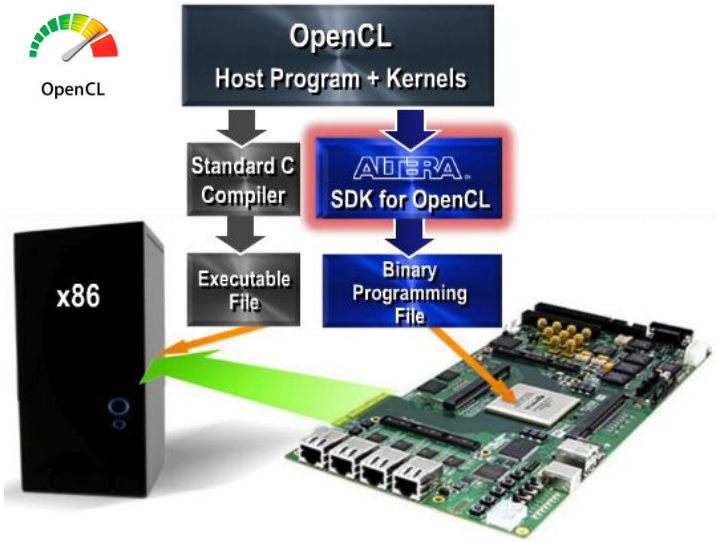
Handy solutions for simple digital circuitry
High Performance Computing
Energy-efficient solutions
High-capability FPGAs
Last couple of years in HPC

http://www.edn.com/electronics-products/other/4413541/SDK-for-OpenCL-helps-software-engineers-harness-FPGA-performance

Role Shift



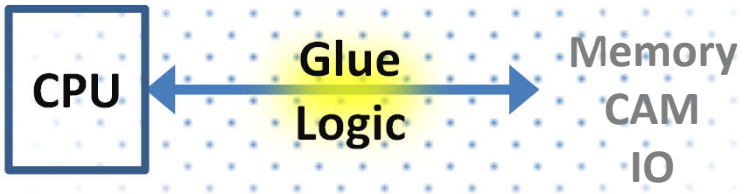
SDK for OpenCL helps software engineers harness FPGA performance - EDN 2013



Handy solutions for simple digital circuitry
High Performance Computing
Energy-efficient solutions
High-capability FPGAs
Last couple of years in HPC

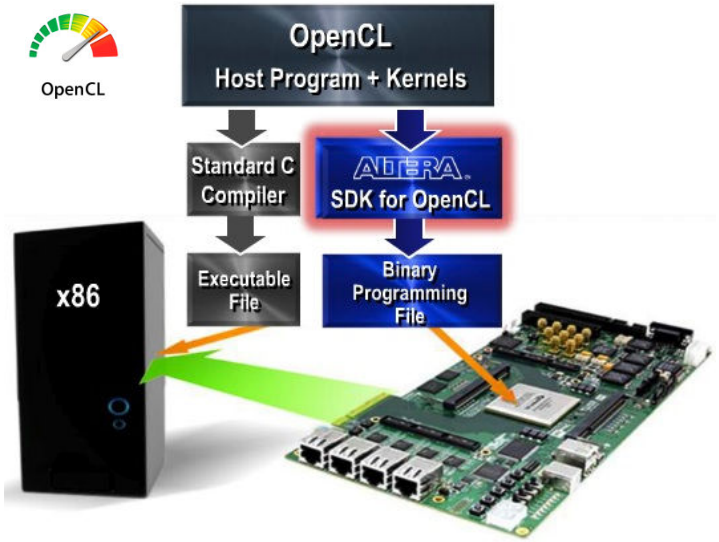
http://www.edn.com/electronics-products/other/4413541/SDK-for-OpenCL-helps-software-engineers-harness-FPGA-performance

Role Shift



SDK for OpenCL helps software engineers harness FPGA performance - EDN 2013

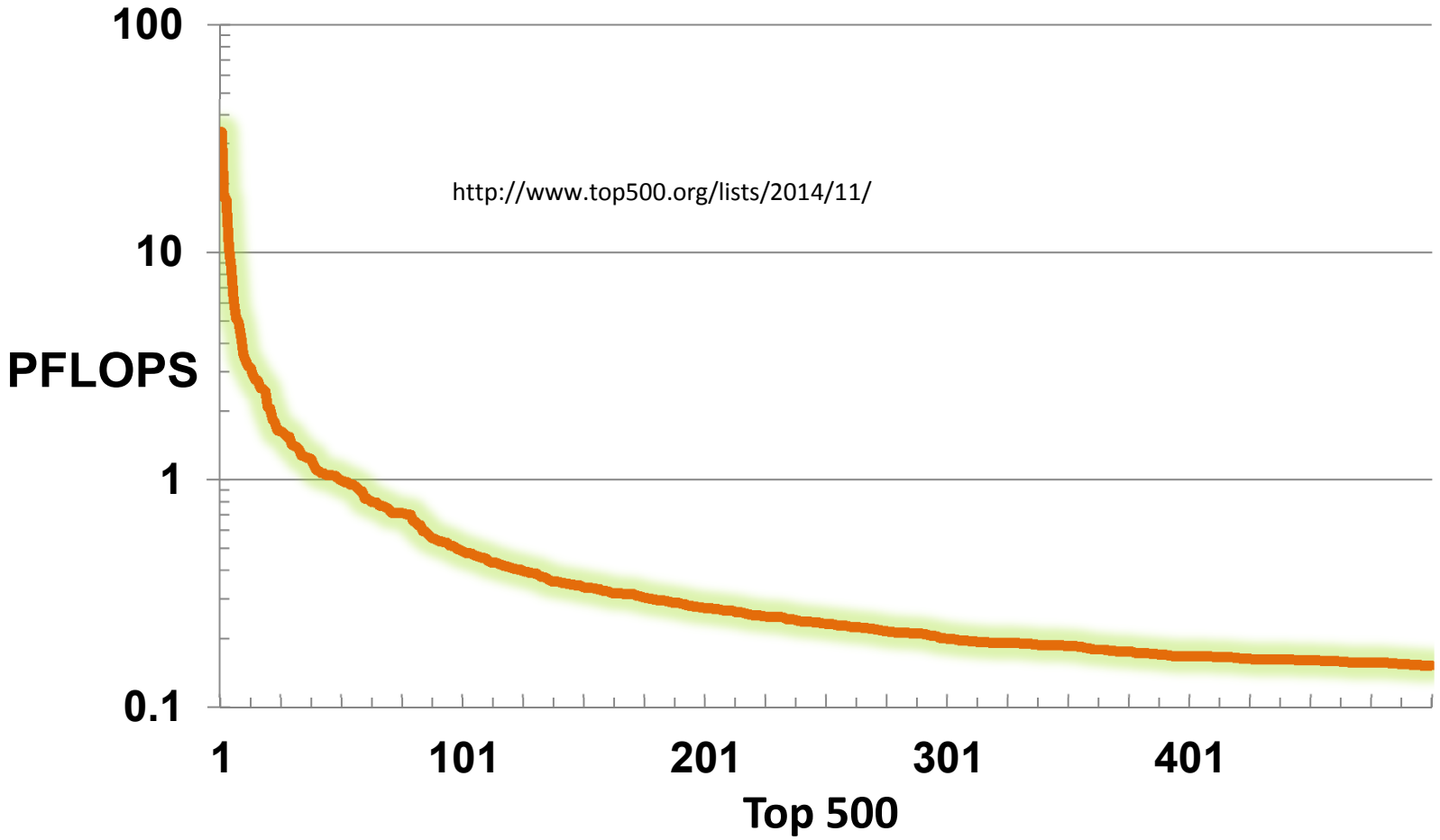
EARLY DAYS → **NOW**



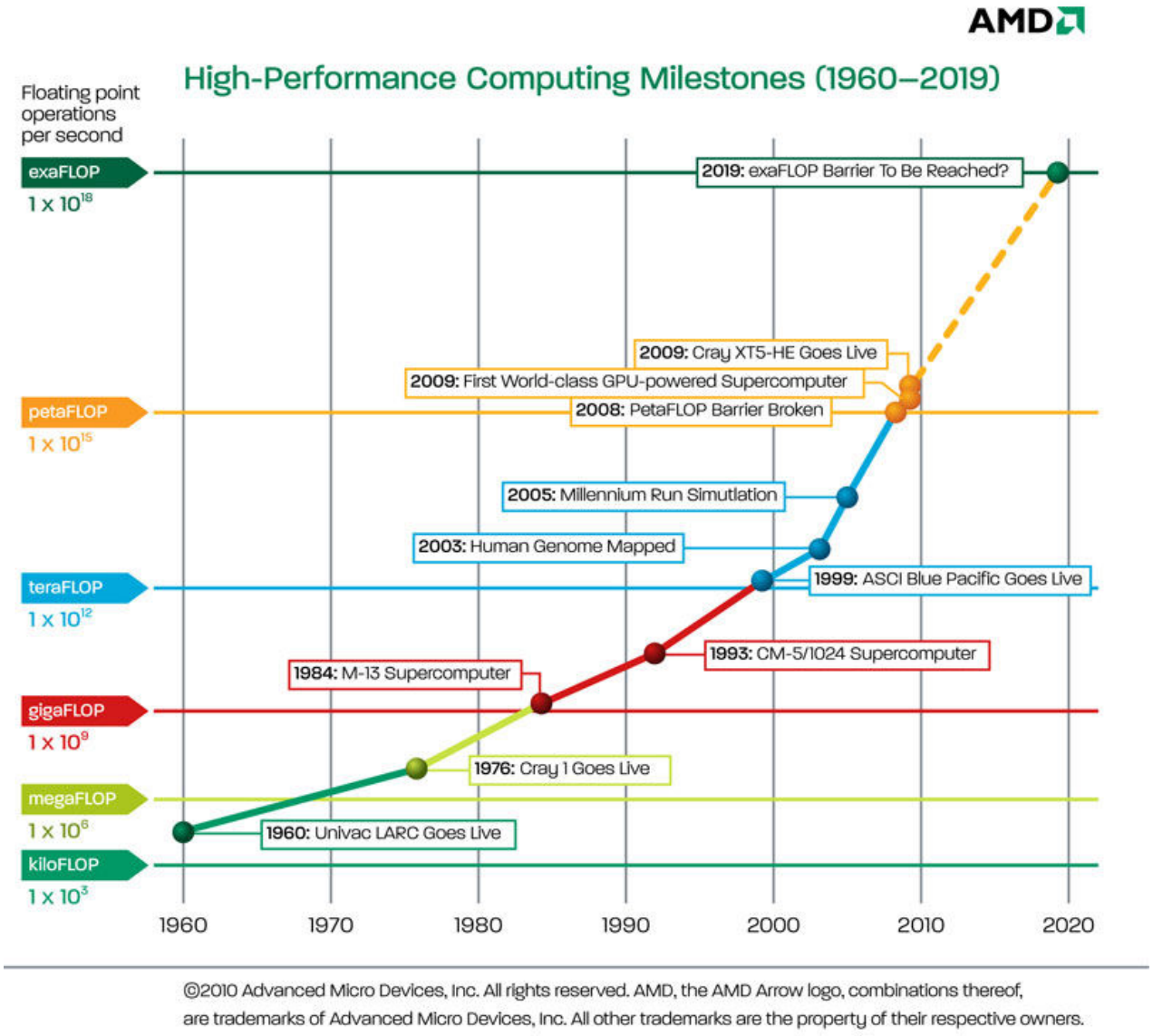
Open Standard for Heterogeneous systems
2008 - OpenCL 1.0 - Now 2.1
FPGA vendors support
Host – Device
FPGA for HPC
Accelerators

http://www.edn.com/electronics-products/other/4413541/SDK-for-OpenCL-helps-software-engineers-harness-FPGA-performance

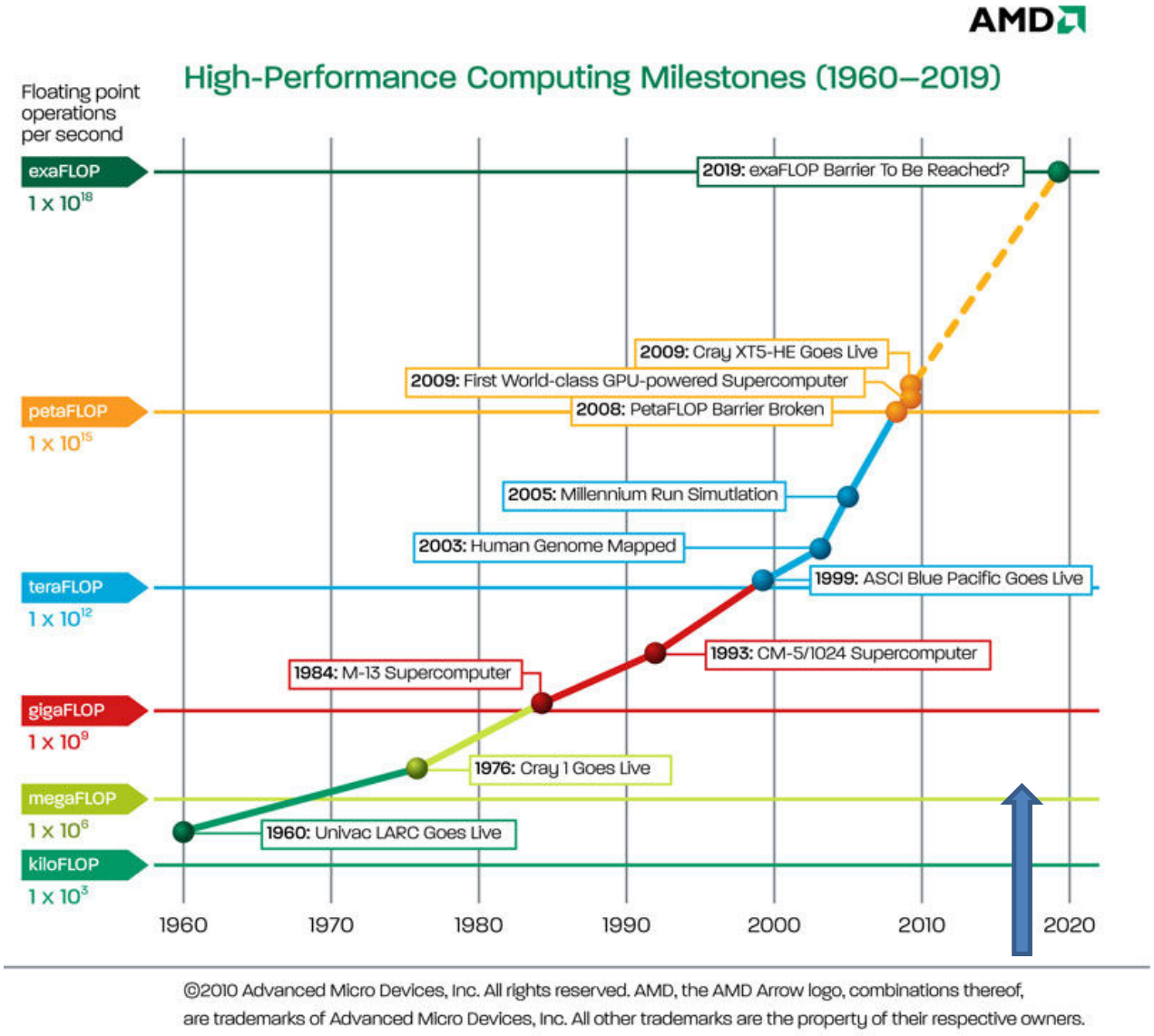
TOP 500
November 2014



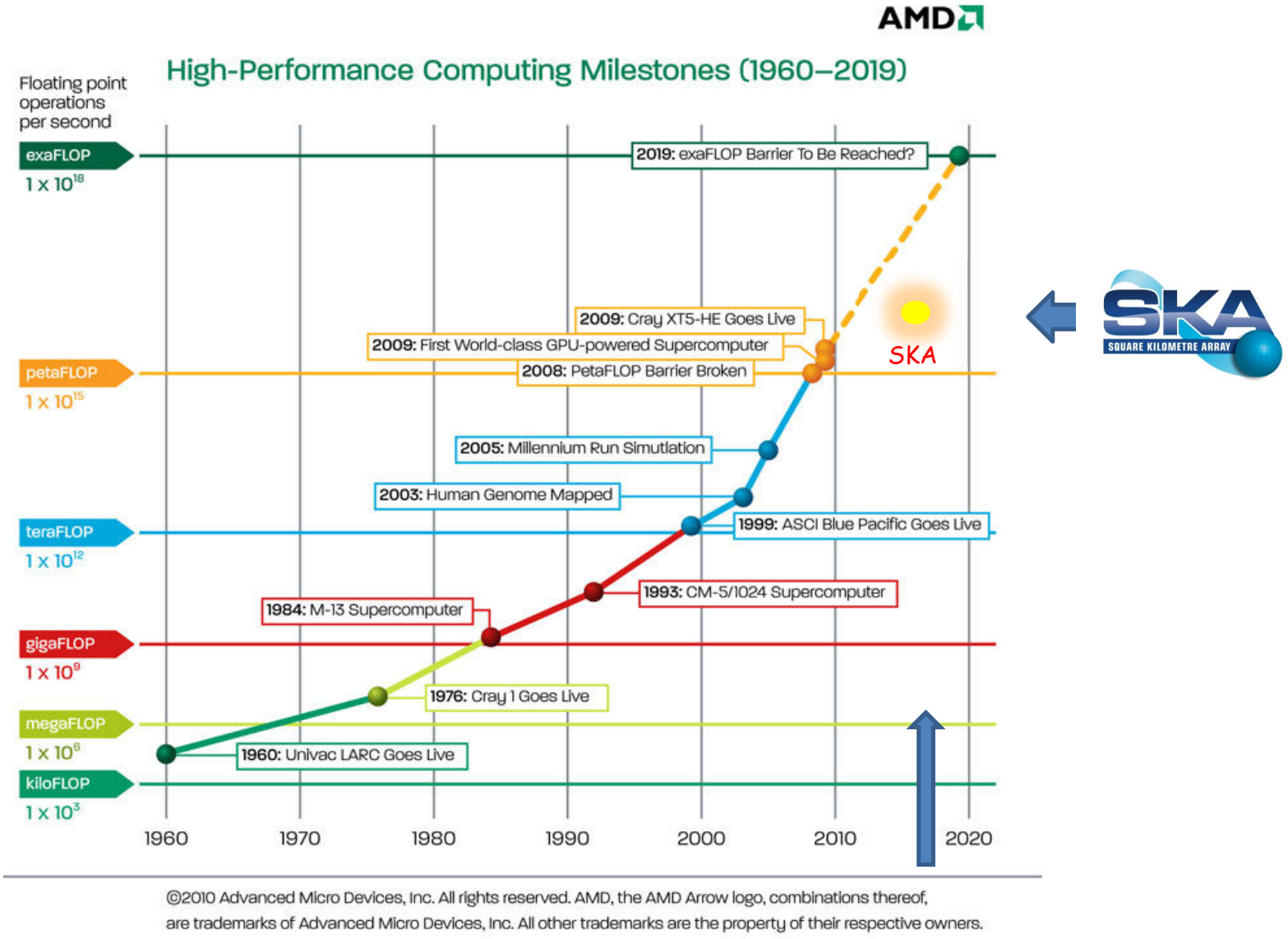
HPC Performance Milestones



HPC Performance Milestones and SKA



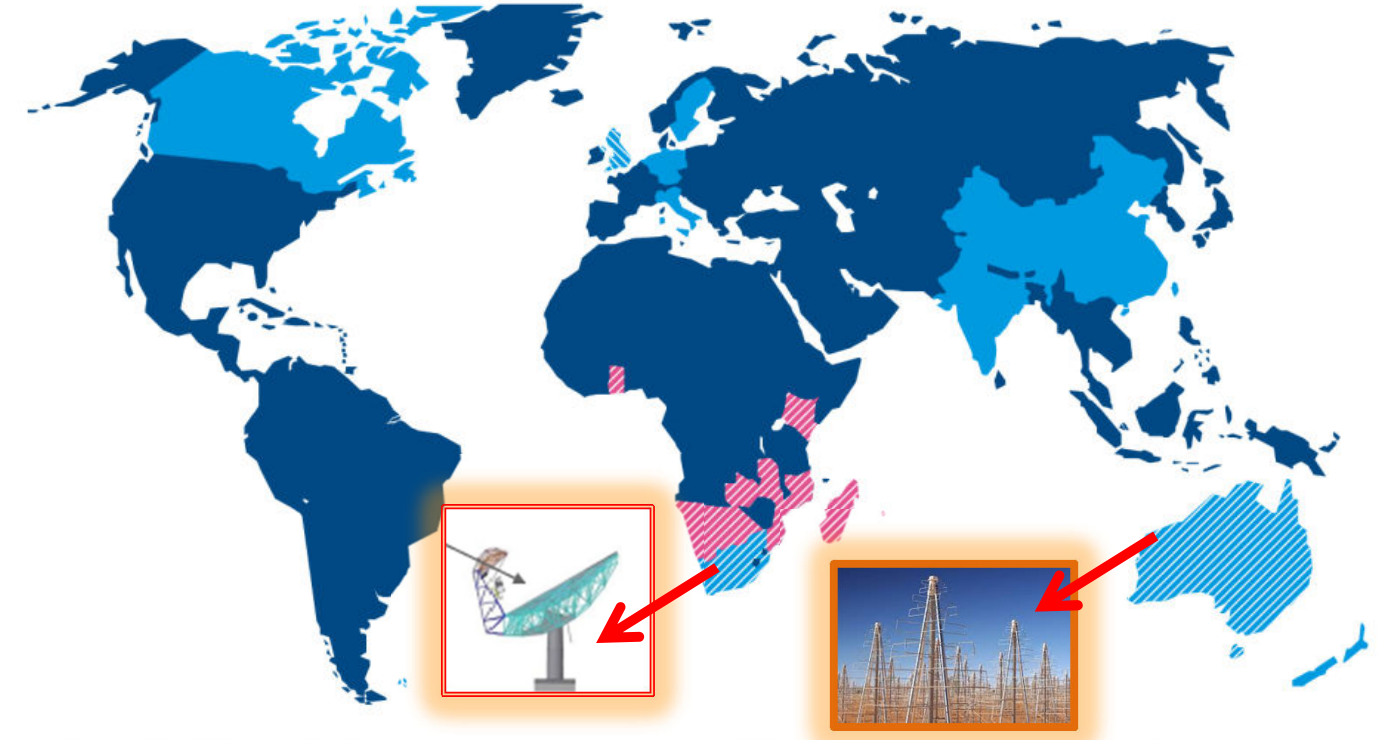
HPC Performance Milestones and SKA



SKA
SQUARE KILOMETRE ARRAY

Square Kilometre Array

A massive Radio Telescope



Full members

SKA Headquarters host country

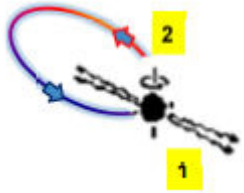
SKA Phase 1 and Phase 2 host countries

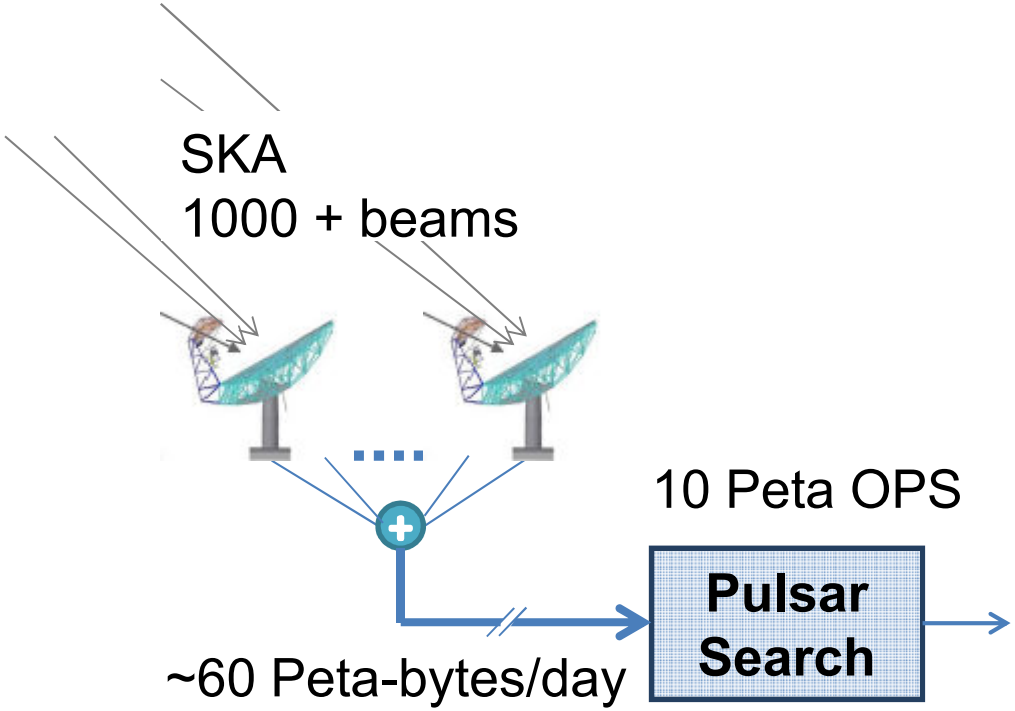
African partner countries
(non-member SKA Phase 2 host countries)

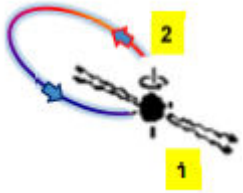
This map is intended for reference only and is not meant to represent legal borders

Pulsar search with SKA

Requires a powerful computing solution.

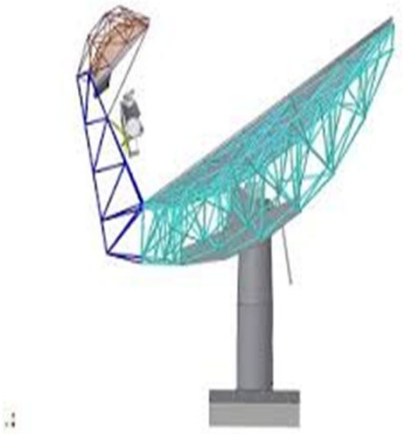


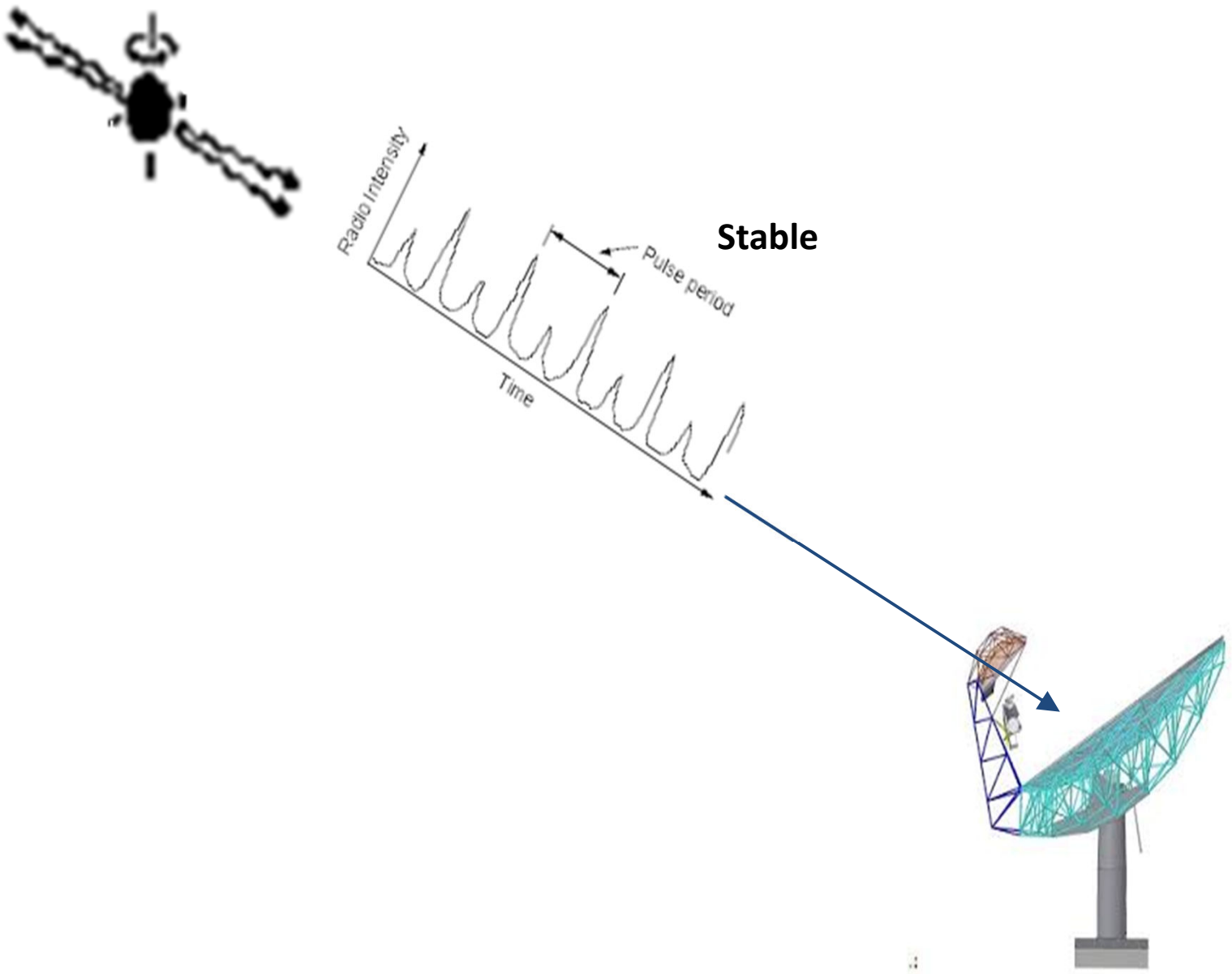


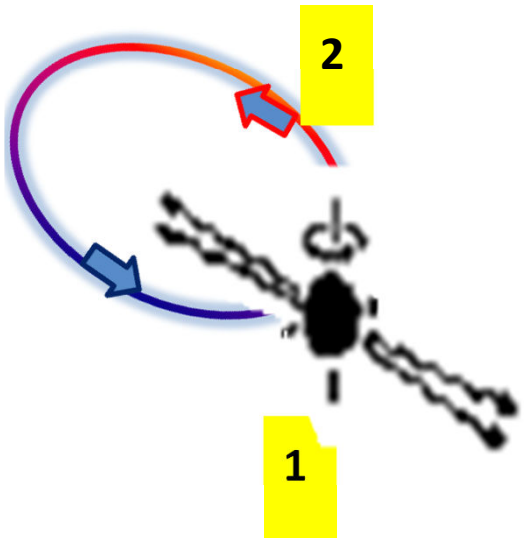


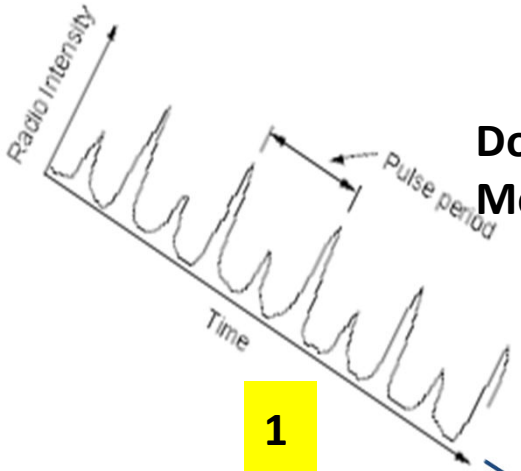
Pulsar Search with SKA

- First Discovery - 1967
- Highly magnetized
- Rotating celestial objects
- Extreme physical nature
- So far about 2400 seen
- Small fraction of the Population
- Powerful Telescope can detect more
- SKA will detect many thousands
- Real time processing

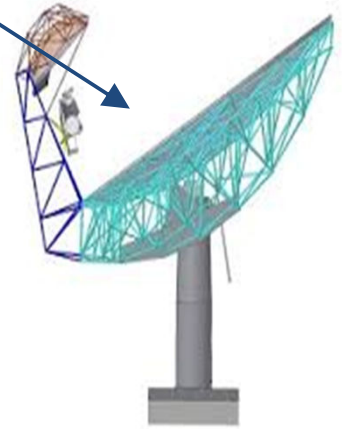


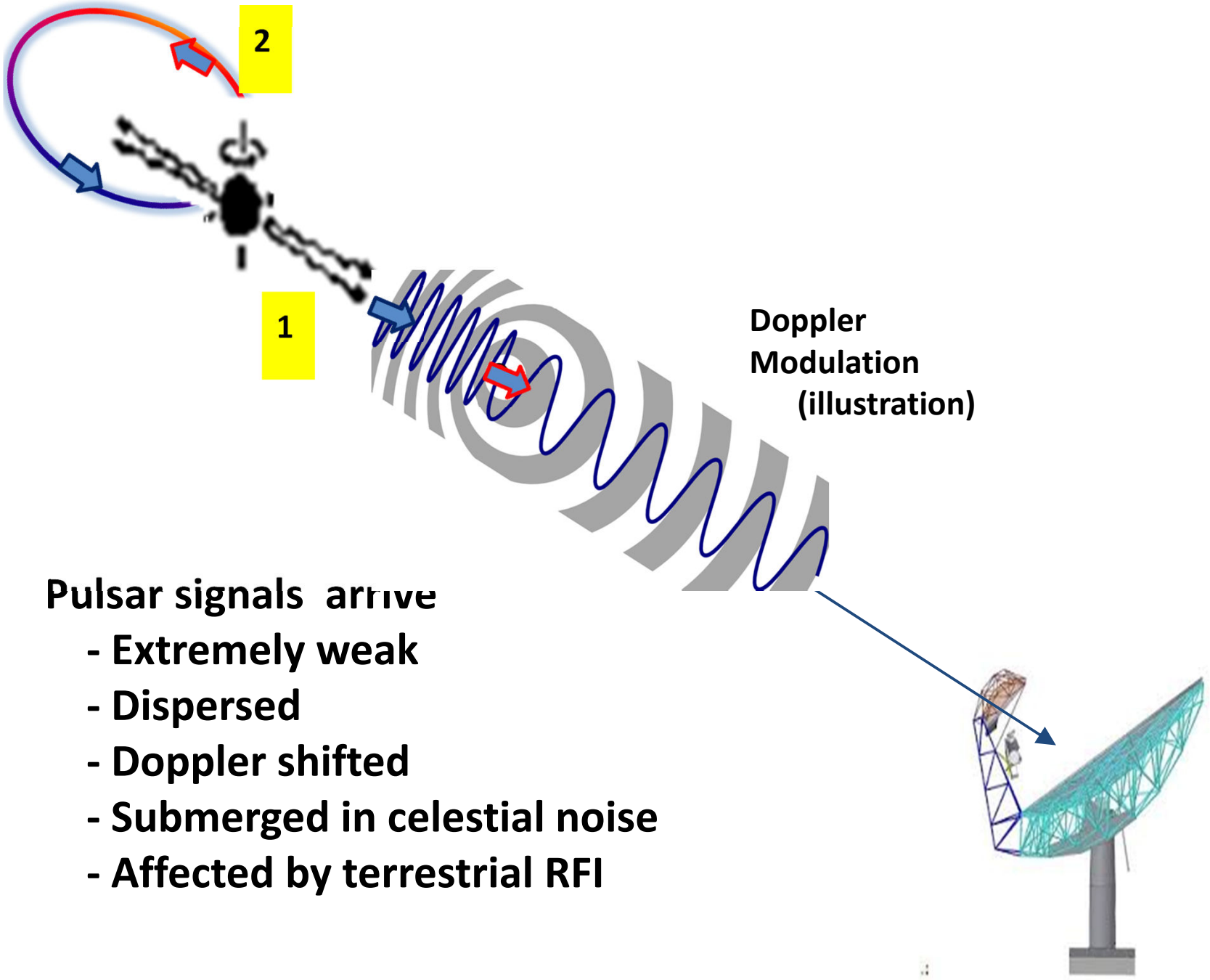

Radio Intensity
Pulse period
Time
Stable





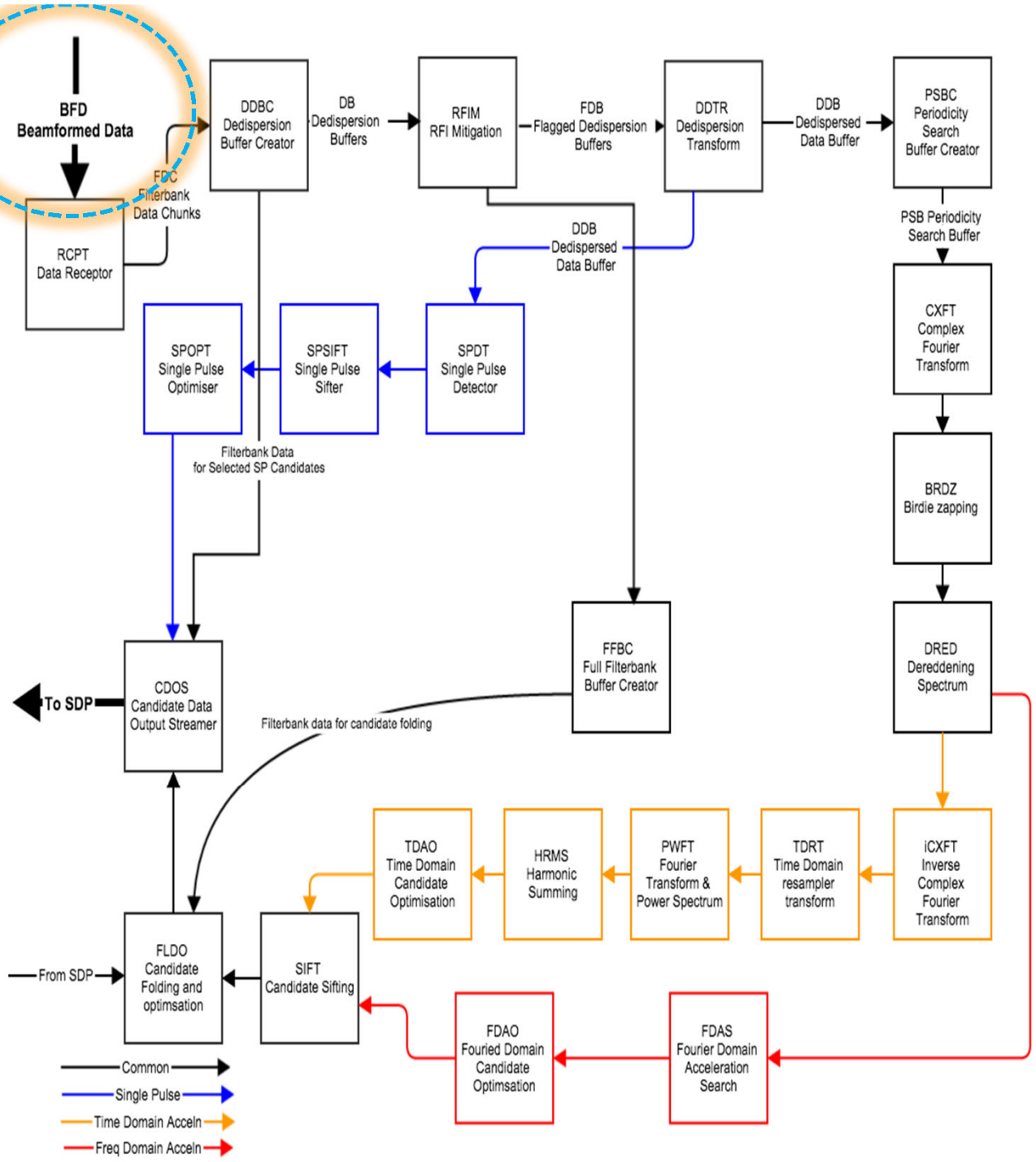
Doppler Modulation **2**

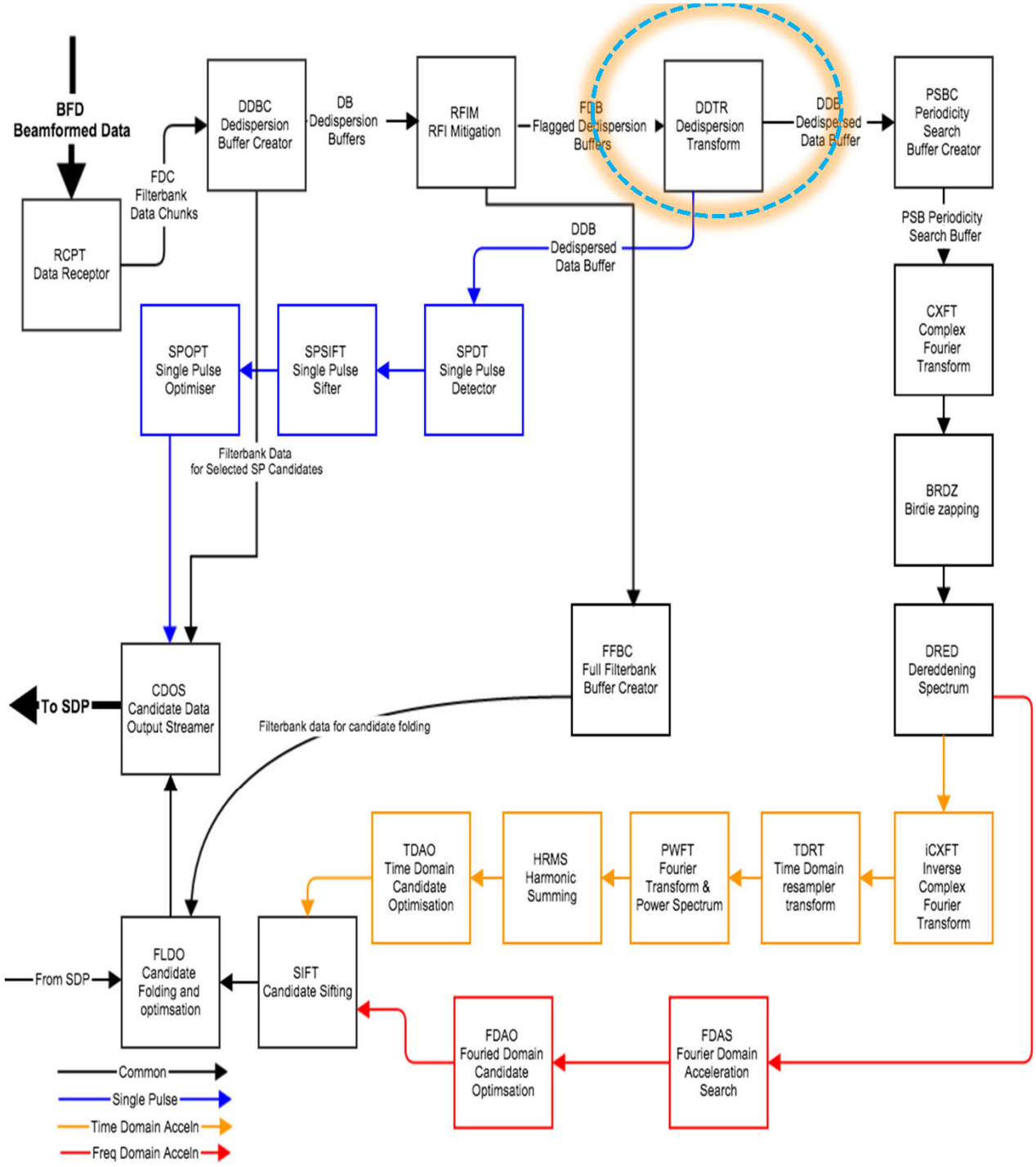


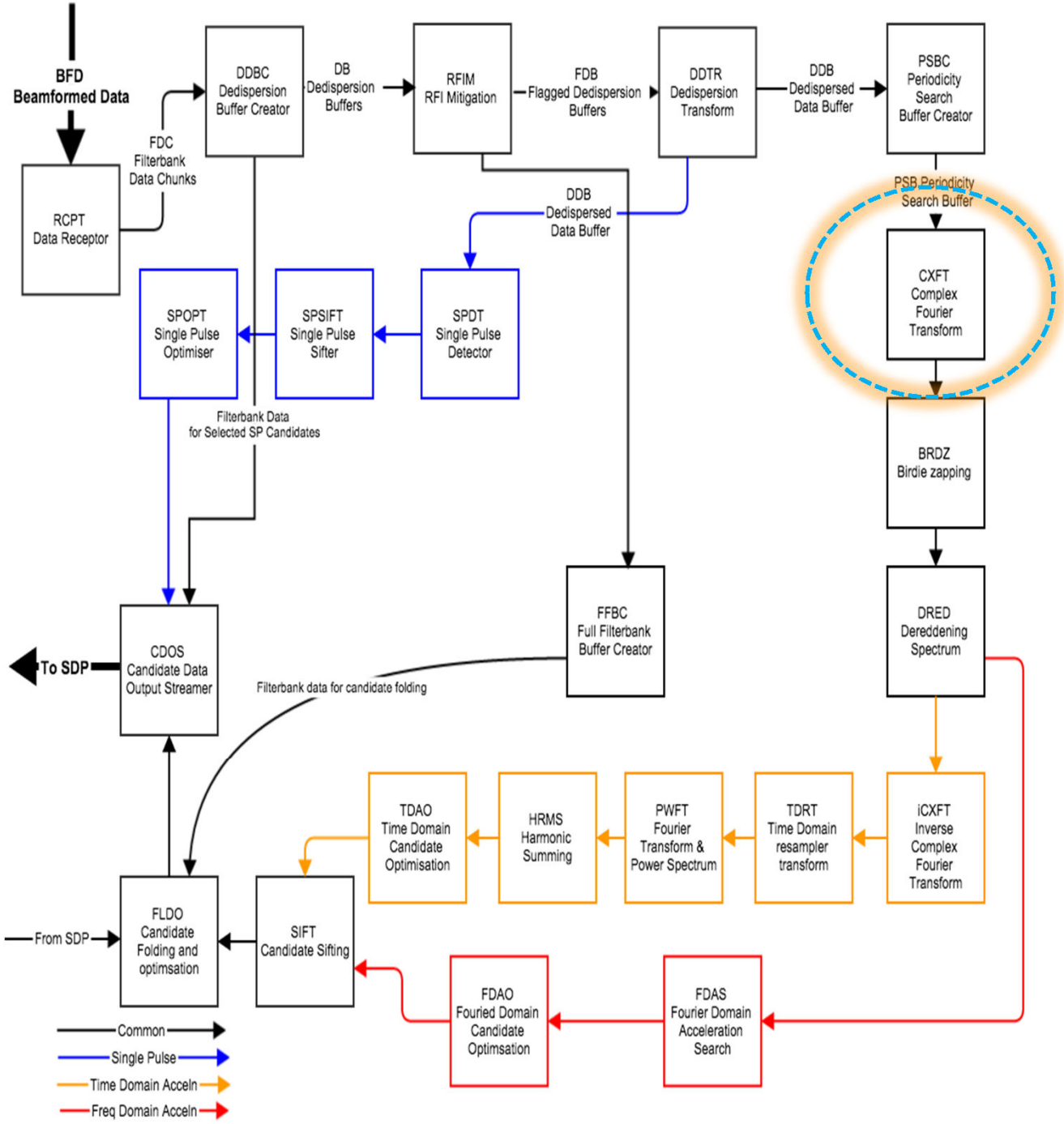


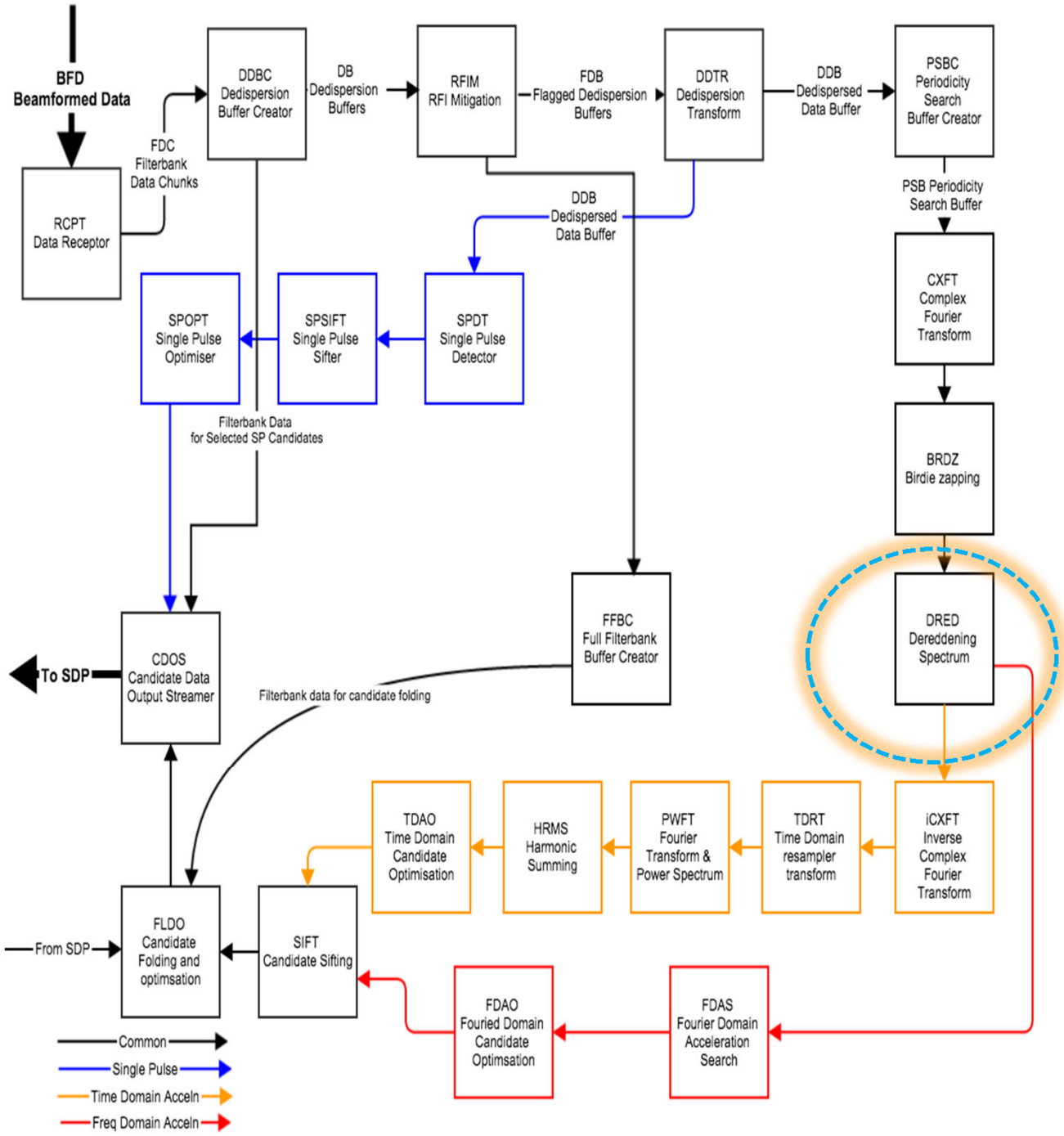
Pulsar signals arrive

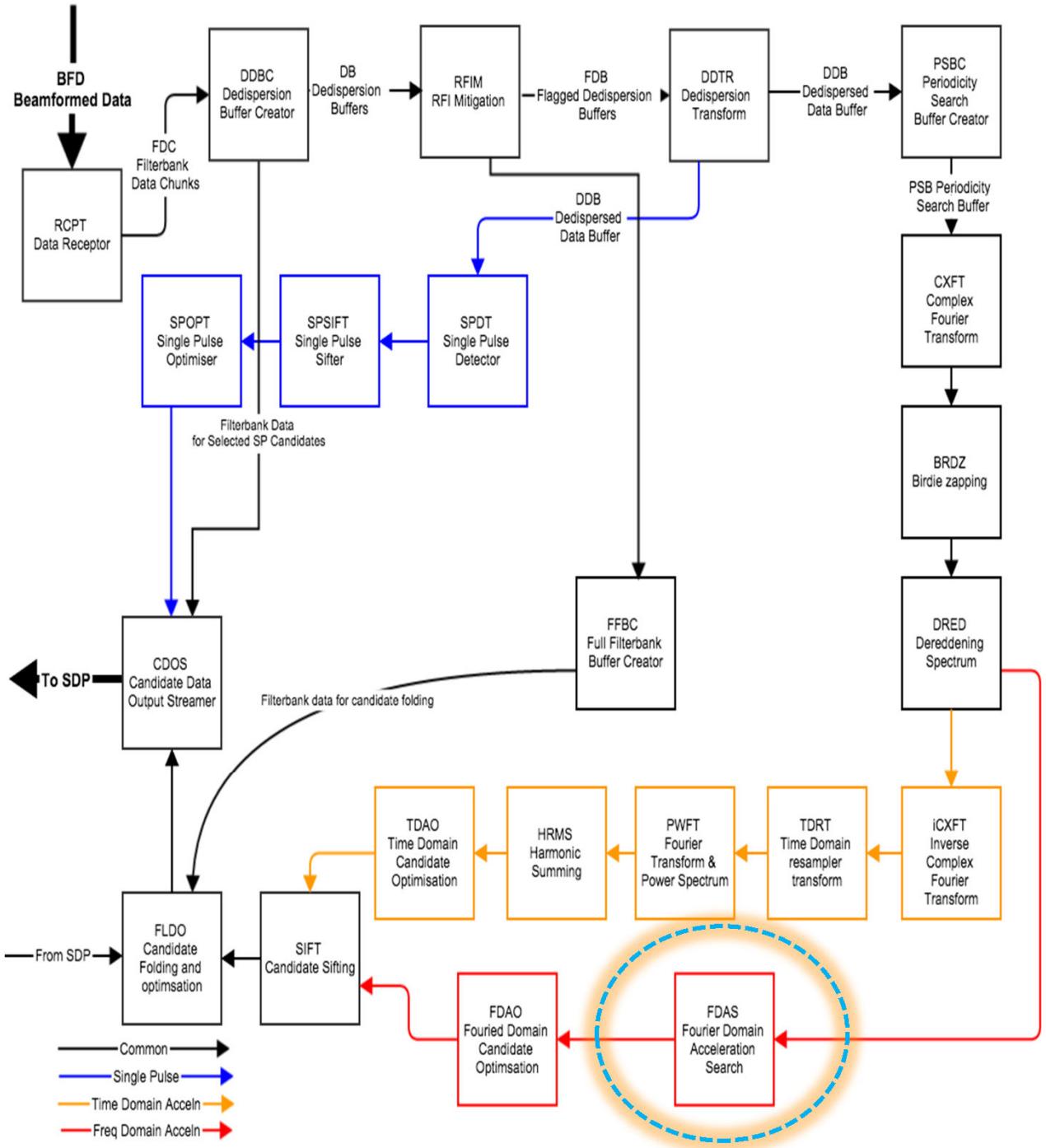
- Extremely weak
- Dispersed
- Doppler shifted
- Submerged in celestial noise
- Affected by terrestrial RFI

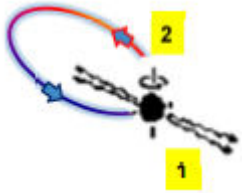

BFD
Beamformed Data
RCPT
Data Receptor
FDC
Filterbank
Data Chunks
DDBC
Dedispersion
Buffer Creator
DB
Dedispersion
Buffers
RFIM
RFI Mitigation
FDB
Flagged Dedispersion
Buffers
DDTR
Dedispersion
Transform
DDB
Dedispersed
Data Buffer
PSBC
Periodicity
Search
Buffer Creator
PSB Periodicity
Search Buffer
CXFT
Complex
Fourier
Transform
BRDZ
Birdie zapping
DRED
Dereddening
Spectrum
iCXFT
Inverse
Complex
Fourier
Transform
TDRT
Time Domain
resampler
transform
PWFT
Fourier
Transform &
Power Spectrum
HRMS
Harmonic
Summing
TDAO
Time Domain
Candidate
Optimisation
DDB
Dedispersed
Data Buffer
SPDT
Single Pulse
Detector
SPSIFT
Single Pulse
Sifter
SPOPT
Single Pulse
Optimiser
Filterbank Data
for Selected SP Candidates
FFBC
Full Filterbank
Buffer Creator
Filterbank data for candidate folding
To SDP
CDOS
Candidate Data
Output Streamer
From SDP
FLDO
Candidate
Folding and
optimsation
SIFT
Candidate Sifting
FDAO
Fouried Domain
Candidate
Optimsation
FDAS
Fourier Domain
Acceleration
Search
Common
Single Pulse
Time Domain Acceln
Freq Domain Acceln


BFD
Beamformed Data
RCPT
Data Receptor
FDC
Filterbank
Data Chunks
DDBC
Dedispersion
Buffer Creator
DB
Dedispersion
Buffers
RFIM
RFI Mitigation
Flagged Dedispersion
Buffers
DDTR
Dedispersion
Transform
DDB
Dedispersed
Data Buffer
PSBC
Periodicity
Search
Buffer Creator
PSB Periodicity
Search Buffer
CXFT
Complex
Fourier
Transform
BRDZ
Birdie zapping
DRED
Dereddening
Spectrum
iCXFT
Inverse
Complex
Fourier
Transform
TDRT
Time Domain
resampler
transform
PWFT
Fourier
Transform &
Power Spectrum
HRMS
Harmonic
Summing
TDAO
Time Domain
Candidate
Optimisation
SIFT
Candidate Sifting
FLDO
Candidate
Folding and
optimsation
From SDP
FDAS
Fourier Domain
Acceleration
Search
FDAO
Fouried Domain
Candidate
Optimsation
DDB
Dedispersed
Data Buffer
SPDT
Single Pulse
Detector
SPSIFT
Single Pulse
Sifter
SPOPT
Single Pulse
Optimiser
Filterbank Data
for Selected SP Candidates
FFBC
Full Filterbank
Buffer Creator
Filterbank data for candidate folding
CDOS
Candidate Data
Output Streamer
To SDP
Common
Single Pulse
Time Domain Acceln
Freq Domain Acceln


BFD
Beamformed Data
RCPT
Data Receptor
FDC
Filterbank
Data Chunks
DDBC
Dedispersion
Buffer Creator
DB
Dedispersion
Buffers
RFIM
RFI Mitigation
FDB
Flagged Dedispersion
Buffers
DDTR
Dedispersion
Transform
DDB
Dedispersed
Data Buffer
PSBC
Periodicity
Search
Buffer Creator
PSB Periodicity
Search Buffer
CXFT
Complex
Fourier
Transform
BRDZ
Birdie zapping
DRED
Dereddening
Spectrum
iCXFT
Inverse
Complex
Fourier
Transform
TDRT
Time Domain
resampler
transform
PWFT
Fourier
Transform &
Power Spectrum
HRMS
Harmonic
Summing
TDAO
Time Domain
Candidate
Optimisation
DDB
Dedispersed
Data Buffer
SPDT
Single Pulse
Detector
SPSIFT
Single Pulse
Sifter
SPOPT
Single Pulse
Optimiser
Filterbank Data
for Selected SP Candidates
FFBC
Full Filterbank
Buffer Creator
Filterbank data for candidate folding
To SDP
CDOS
Candidate Data
Output Streamer
From SDP
FLDO
Candidate
Folding and
optimsation
SIFT
Candidate Sifting
FDAO
Fouried Domain
Candidate
Optimsation
FDAS
Fourier Domain
Acceleration
Search
Common
Single Pulse
Time Domain Acceln
Freq Domain Acceln


BFD
Beamformed Data
RCPT
Data Receptor
FDC
Filterbank
Data Chunks
DDBC
Dedispersion
Buffer Creator
DB
Dedispersion
Buffers
RFIM
RFI Mitigation
FDB
Flagged Dedispersion
Buffers
DDTR
Dedispersion
Transform
DDB
Dedispersed
Data Buffer
PSBC
Periodicity
Search
Buffer Creator
PSB Periodicity
Search Buffer
CXFT
Complex
Fourier
Transform
BRDZ
Birdie zapping
DRED
Dereddening
Spectrum
iCXFT
Inverse
Complex
Fourier
Transform
TDRT
Time Domain
resampler
transform
PWFT
Fourier
Transform &
Power Spectrum
HRMS
Harmonic
Summing
TDAO
Time Domain
Candidate
Optimisation
SIFT
Candidate Sifting
FLDO
Candidate
Folding and
optimsation
From SDP
FDAS
Fourier Domain
Acceleration
Search
FDAO
Fouried Domain
Candidate
Optimsation
DDB
Dedispersed
Data Buffer
SPDT
Single Pulse
Detector
SPSIFT
Single Pulse
Sifter
SPOPT
Single Pulse
Optimiser
Filterbank Data
for Selected SP Candidates
FFBC
Full Filterbank
Buffer Creator
Filterbank data for candidate folding
CDOS
Candidate Data
Output Streamer
To SDP
Common
Single Pulse
Time Domain Acceln
Freq Domain Acceln

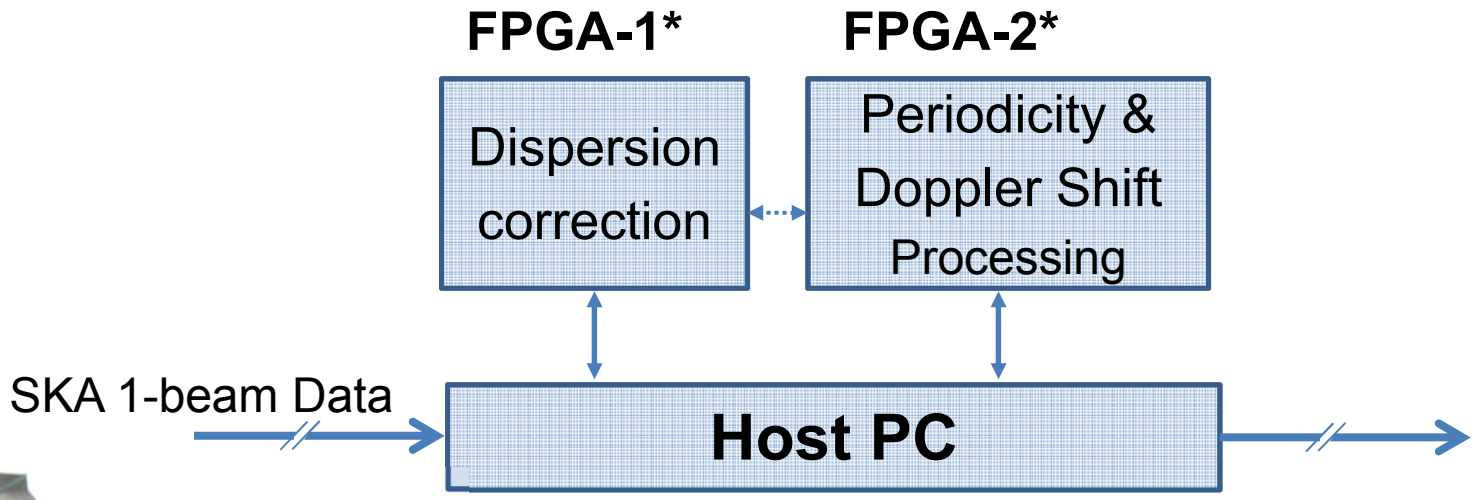

BFD
Beamformed Data
RCPT
Data Receptor
FDC
Filterbank
Data Chunks
DDBC
Dedispersion
Buffer Creator
DB
Dedispersion
Buffers
RFIM
RFI Mitigation
FDB
Flagged Dedispersion
Buffers
DDTR
Dedispersion
Transform
DDB
Dedispersed
Data Buffer
PSBC
Periodicity
Search
Buffer Creator
PSB Periodicity
Search Buffer
CXFT
Complex
Fourier
Transform
BRDZ
Birdie zapping
DRED
Dereddening
Spectrum
iCXFT
Inverse
Complex
Fourier
Transform
TDRT
Time Domain
resampler
transform
PWFT
Fourier
Transform &
Power Spectrum
HRMS
Harmonic
Summing
TDAO
Time Domain
Candidate
Optimisation
DDB
Dedispersed
Data Buffer
SPDT
Single Pulse
Detector
SPSIFT
Single Pulse
Sifter
SPOPT
Single Pulse
Optimiser
Filterbank Data
for Selected SP Candidates
FFBC
Full Filterbank
Buffer Creator
Filterbank data for candidate folding
To SDP
CDOS
Candidate Data
Output Streamer
From SDP
FLDO
Candidate
Folding and
optimsation
SIFT
Candidate Sifting
FDAO
Fouried Domain
Candidate
Optimsation
FDAS
Fourier Domain
Acceleration
Search
Common
Single Pulse
Time Domain Acceln
Freq Domain Acceln

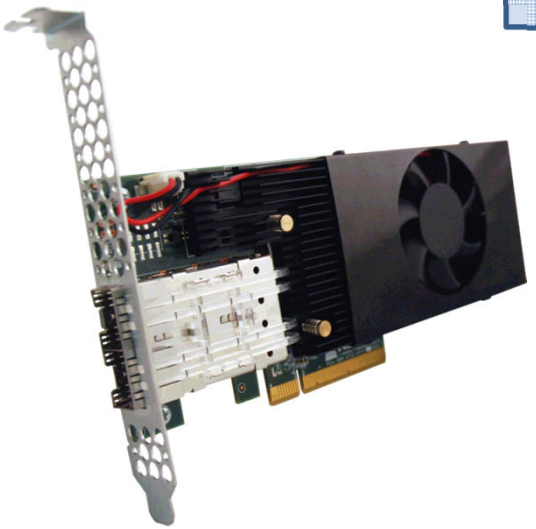


FPGA HPC for Pulsar Search with SKA

We are evaluating an FPGA-based HPC solution to search for pulsars with Square Kilometre Array (SKA) telescope

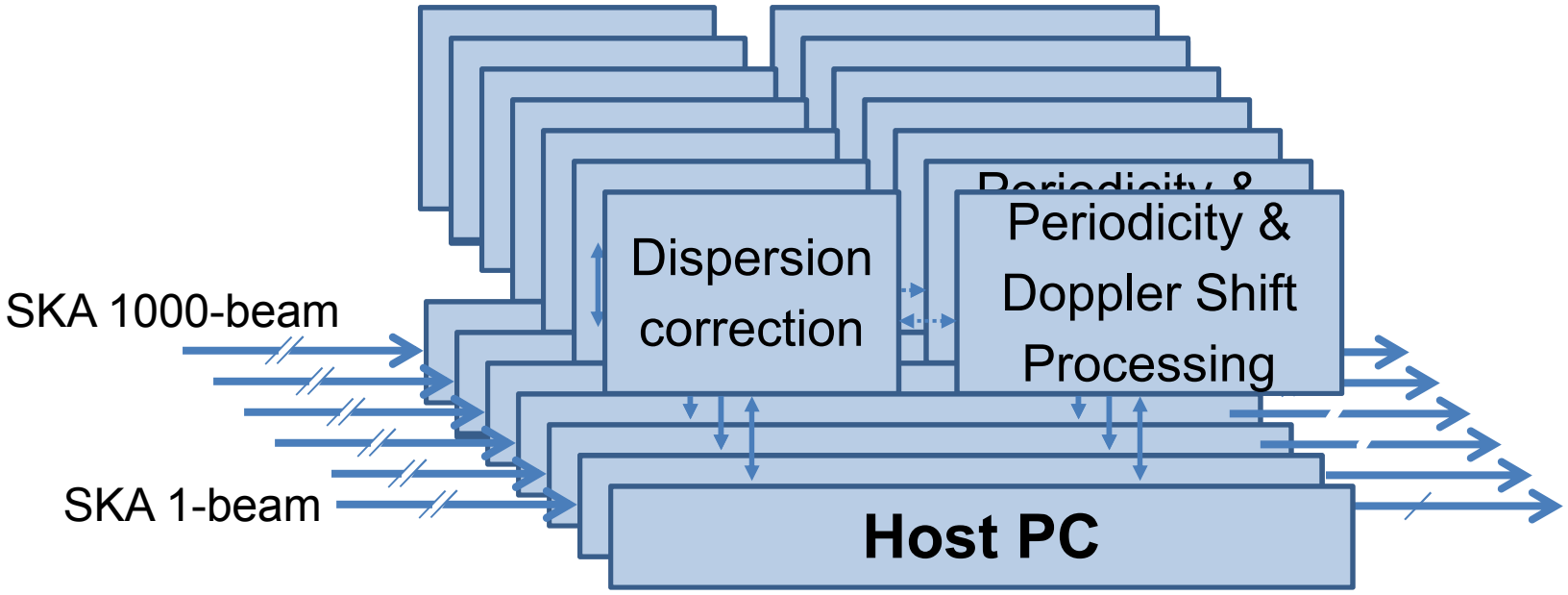
An FPGA based HPC





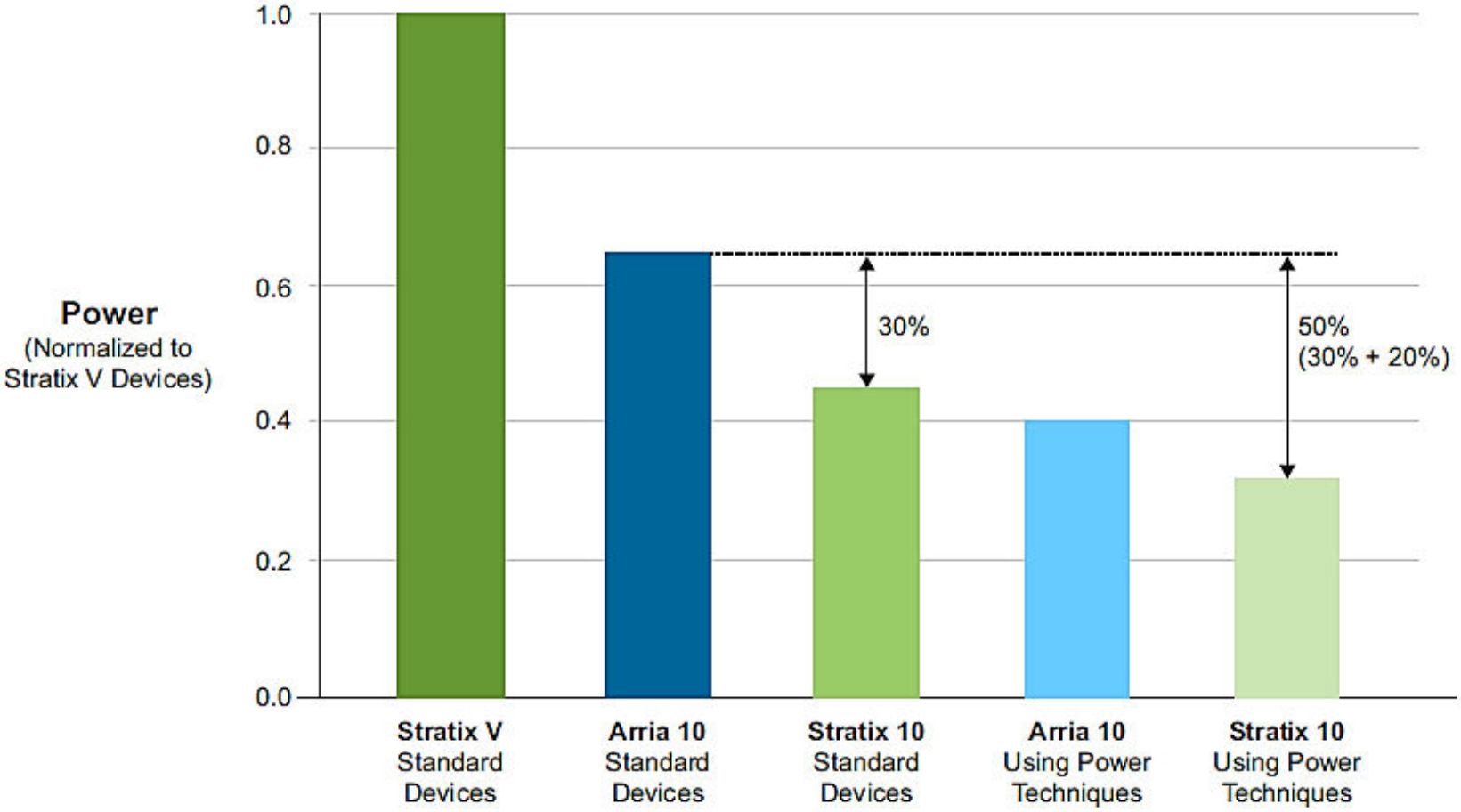
* **Altera Stratix V** P385 D5 based HPC accelerator cards from **Nallatech ®**

A final solution with Multiple FPGA Accelerators

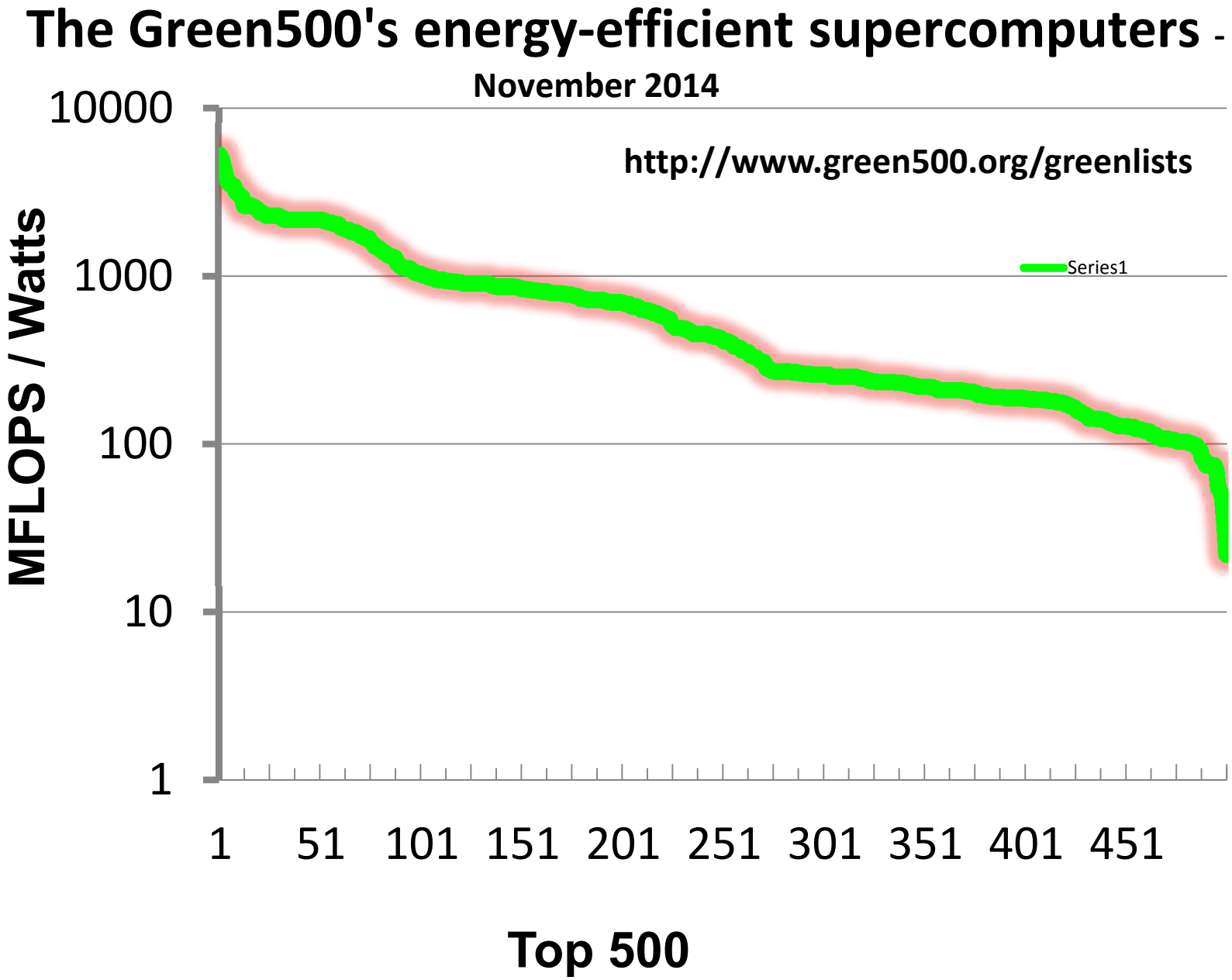


1000+ Beam Processing = 1000+ Node HPC

Power Efficiency in FPGA based HPC



Significant power reduction expected in Altera ® Stratix 10 FPGAs


The Green500's energy-efficient supercomputers -
November 2014
http://www.green500.org/greenlists
Series1
MFLOPS / Watts
10000
1000
100
10
1
1
51
101
151
201
251
301
351
401
451
Top 500

FPGA HPC
Desirable Features

- Fast Compilation
- Incremental Compilation
- Template library support
- Just-in time compilation
- Library pooling
- Partial reconfiguration
- Programming Community

Summary

- Fine-grain Parallelism
- OpenCL & HPC
- SKA Pulsar search
- Power Performance

Acknowledgements:

JBCA, SKA PSS Group, Altera ®, Nallatech ®

Thank You


EMiT
Emerging Technology Conference
2015
MANCHESTER
1824
The University of Manchester